Fabrication and Characterization of GeS Field Effect Transistors

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Abstract:

In previous work (Zhang et al.) was able to successfully demonstrate the use of GeS in Field Effect Transistors (FETs). The performance of the devices was of poor quality which can be observed from the I-V plots. This can be attributed to high contact resistance caused by fermi-level pinning (Sun et al.) and poor growth of GeS thin films using (Chemical Vapor Deposition) CVD. The high contact resistance can be solved by choosing a metal whose work function is much closer to GeS (φ_{GeS}= 5.6eV, φ_{Pd}= 5.5-5.8eV (Merrick et al.). The quality of the grown GeS can be improved by using a seed layer of Al_2O_3 to promote greater nucleation sites and uniform crystallinity across the substrate (Rammula et al.). The focus of this study to investigate the change in performance parameters such as On-Off ratio and Carrier Mobility of GeS FETs.

Summary of Research:

Miniaturization of FETs has long been the way to increase the performance of Si based transistors, but they have led to variety of issues in recent times as the gate oxide thickness and channel length decrease. Low carrier mobility of Si sub 2nm have set a physical limit to how small they can be. Increased gate leakage current has led to heating issues and quantum mechanical effects have led to unpredictable behavior of devices. While some of these issues can be engineered to follow the trend of miniaturization, scientists are looking at other materials to meet the demands of technology.

2-D materials have high carrier mobility at sub 2nm and a Van der Waals (VdW) gap that prevent interstitial defects in suppressing current injection. Researchers have used TMDs such WeS_2 and $MoSe_2$ (Lee et al, Radisavljavic et al.) and demonstrated their functionality in FETs. Not much work has been done in investigating Group IV monochalcogenides such as GeS even though theoretical calculations find that its

carrier mobility is 10 times that of MoS_2 (Yang et al.). GeS has an indirect bandgap of 1.6eV, spin–orbit interactions and lower growth temperatures to TMDs making it suitable for optoelectronic applications.

Methods:

A 20nm layer of Al_2O_3 is grown on a SiO_2 substrate using Atomic Layer Deposition (ALD) by using Trimethylaluminum (TMA) as a precursor. Then CVD of GeS is carried out following the methods of Zhang et al. We then spincoat the substrate using a positive photoresist of OFPR800 at 5000 rpm for 60 sec to achieve a resist thickness of 1.2um. Pre-exposure bake at 90C for 3mins and then laser exposure at 90mj/cm2 (Designs were created in QCAD and laser lithography on DL-1000). Develop in a solution of 2.35% Tetramethylammonium Hydroxide (TMAH) for 90sec and then rinse in de-ionized water for 60 secs in separate baths. Etch away the unwanted GeS to create channels using Inductively Coupled Reactive Ion Etching (ICP-RIE) using CF_4 gas for 120secs at an RF Power of 100W (etching done on CE-300I). The damaged layer of resist is removed by H_2O plasma for 1min (plasma done on AQ-500). The sample is then spin coated with PMGI SF_6 with a pre-exposure bake at 180C for 3mins and OFPR 800 (same recipe as first spin coating), both at 5000rpm for 60 secs. Laser lithography of electrodes is carried out. It is developed in TMAH (2.35%) for 60 secs and rinsed in water baths as previous development recipe. The sample is then deposited with 3nm of Pd and 50nm of Au using electron beam evaporation. Lift-off is carried out in NMP at 80C for 1hr followed by washings in Acetone (3 times) and IPA. Raman spectroscopy (532nm laser was used) of the GeS is conducted to check the quality of the semi-conducting channel and subsequently two-probe measurements are completed to extract the transfer characteristics of the devices. Surface Dektak profiler was used to check for surface defects during the fabrication process. The final device stack is depicted in Fig. 1.

Conclusions and Future Steps:

We were able to improve On-off ratio by 5 times and carrier mobility by 2 times. The theoretical limit of

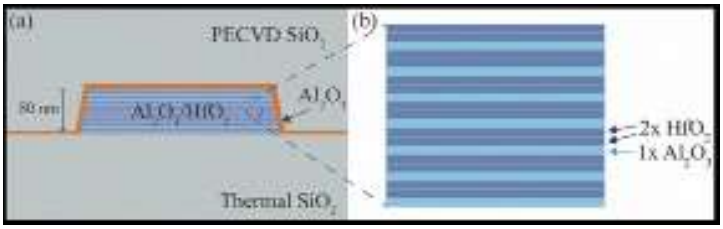

Figure 1: Waveguide cross-section showing an HfO_2-based core, a 4 nm thick Al_2O_3 diffusion barrier and PECVD SiO_2 cladding.

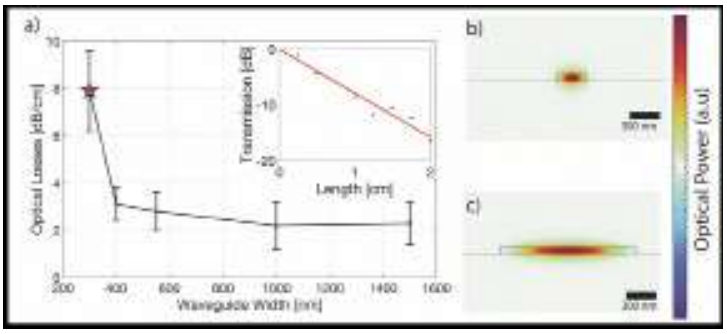

Figure 2: Optical micrograph of a representative device used to measure optical losses. To the right, an SEM image of a grating coupler used to couple light into the device.

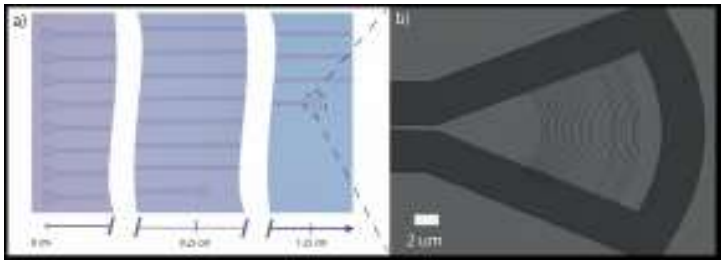

Figure 3: Measured optical losses for varying widths at 375 nm. Inset shows data obtained for a width of 300 nm.

carrier mobility in GeS was not achieved, which suggests Fermi-level pinning is independent of the work function of the metal and presence of surface defects is suspected and alternate strategies to create ohmic contacts must be studied further. The improvement of on-off ratios and subthreshold swing suggests that the growth of GeS on a seed layer promotes greater crystalline growth. The GeS substrate had larger nucleation sites compared to previous studies but was still discontinuous and non-uniform in thickness as confirmed by surface measurements. The carrier mobility extraction was done using two-probe measurements which give a rough estimate of the value but more sensitive techniques such as four probe measurements/ hall measurements must be employed in the future to isolate the effects of contact resistance. An interesting phenomenon of ferroelectric effect was observed in Fig. 2c which opens up new opportunities for non-volatile memory applications in group-14 monochalcogenides, similar to what has been reported for GeSe by Sui, F et al. Next steps would be to improve CVD of GeS as it seems to be the biggest factor contributing to performance and fabricate devices on thinner gate oxides.

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