

Challenges for Diamond Integrated Circuits

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Abstract:

Diamond is a nontraditional material for use in the transistor industry. It poses many challenges for consistent fabrication over semiconductors such as silicon or gallium arsenide. However, diamond has several desired material characteristics for integrated circuits (ICs). We therefore explored the properties of several simple devices on diamond — namely, transistors, inverters, and ring oscillators.

Introduction:

Integrated circuits developed using silicon technology in the last several decades have radically changed our way of life. However for some applications such as high power or frequency equipment, silicon is not ideal. Diamond with its large band gap and thermal conductivity and bulk insulating properties could be used. In this experiment, we investigated hydrogen terminated diamond [1]. In this case, the last carbon atoms of the diamond were bonded to hydrogen (H). The difference in electronegativity between the carbon and hydrogen atoms yielded a very thin two-dimensional layer of holes that can be used for a transistor channel.

To illustrate the possibilities of ICs on diamond, we attempted to fabricate several simple electronic devices, namely, transistors, logic inverters, and ring oscillators. A transistor is the fundamental building block of ICs that only allows current flow if a voltage is applied to the gate. An important property for device fabrication is that transistors be normally off, or have no current flowing when no voltage is applied to the gate. Inverters simply flip logic high (1) into a logic low (0) and vice versa. Ring oscillators are more complex device made of an odd number inverters connected in a ring. An input signal is then continually flipped from high to low, ideally yielded an output sine wave. To fabricate these devices, we used a process called microlithography, which uses light to ‘draw’ on an optically sensitive material covering the sample.

Experimental Procedure:

The electronic devices were fabricated using a standard sequence of nanofabrication steps.

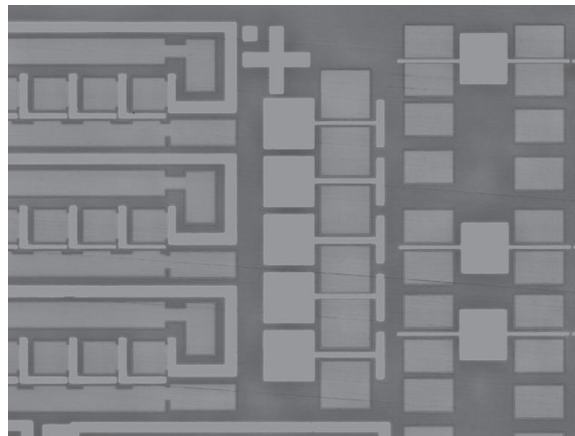


Figure 1: The sample just before the gold source-drain layer was deposited.

First, a square 5 mm H-terminated diamond sample was chosen as the substrate. We used the software Vectorworks to create a layout, measuring 3.5 mm × 4 mm, that was eventually patterned onto the substrate. The patterning process built the devices in a series of layers. The general sequence of steps was spin coat the resist, apply laser lithography, develop, deposit material, and finally liftoff. Once one layer was completed, we systematically moved onto the next.

Photolithography was conducted on a maskless system. Unfortunately our samples were not perfectly flat so the auto-aligning system could not be used. The material deposition step varied based on the layer. For example, the mesa layer consisted of ozone cleaning to strip the hydrogen terminated ends and remove conductivity from the uncovered regions. All other layers deposited a palladium (5nm)/titanium (10nm)/gold (150nm) onto the surface. For the gate region, 30 nm of aluminum oxide was deposited first by atomic layer deposition.

See Figure 1 for a visual representation of the sample, late in the process. Here, lithography and development have already happened for the final layer, so the bare substrate is visible.

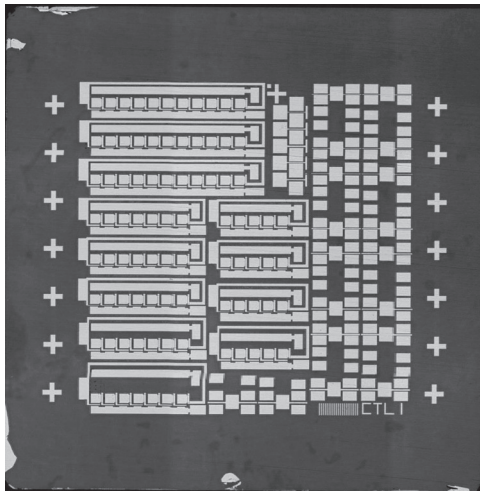


Figure 2: The completed chip with ring oscillators on the left and inverters on the right.

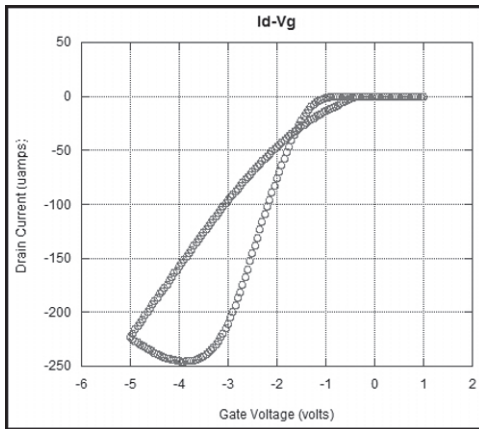


Figure 3: Plot of drain current (I_d) versus gate voltage (V_g), sweeping the voltage in both directions to observe hysteresis.

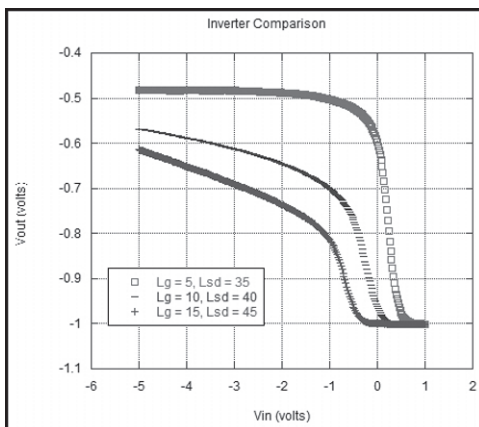


Figure 4: Illustration that inverter operation is more successful for smaller values of gate length.

Results and Conclusions:

We successfully fabricated functioning transistors and inverters on a hydrogen terminated diamond substrate. During the experiment, we fabricated devices in two different orders. In the first batch, they were source-drain first and the second gate first. In theory, the order should not have a large effect on the final functionality of the device. In practice, the normally on/off characteristics were dependent on this order. Depositing the gate first yielded a much higher percentage of normally off devices. This satisfied one of our goals to consistently fabricate normally off devices.

Figure 3 illustrates this using an I_d - V_g graph. Here it is clear that the no current is flowing when zero voltage is applied to the gate. In these transistors, the average drain current achieved was on the order of a milliamp.

A second interesting conclusion can be drawn from Figure 3; there was a major difference in the transistor properties depending on if we swept the gate voltage in forward or reverse. This is known as hysteresis. A possible explanation for this comes from the two-dimensional nature of the charges in the channel, and capture and emission phenomena between holes and defect trap. This may have contributed to the ring oscillators not functioning.

Finally, Figure 4 shows successful inverter operation. Ideal inverters would very sharply transition from high to low voltage. Greater separation between the high and low voltage is also desired. Therefore we observe that inverters with narrower gate lengths perform better. In the same way (graph not pictured), smaller source drain distances perform better. These results were expected because transistors generally perform better at smaller scales.

Future Work:

Possible directions that this research could take in the future include theoretical explanations of the normally off and hysteresis behavior. The causes of these effects are still only loosely understood. There is also a chance that a good model for the hysteresis could facilitate ring oscillator construction.

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References:

- [1] H. Kawarada, et al., Appl. Phys. Lett. 65, 1563-1565 (1994).