

P-channel GaN Transistors on the AlN Platform

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Abstract:

The development of complementary GaN electronics requires high-performance p-channel field-effect transistors (pFETs) capable of matching the on-currents of GaN HEMTs [1]. However, p-GaN devices suffer from low hole mobility and poor dopant activation, resulting in high on-resistance and limited output current. Polarization-engineered GaN/AlN heterostructures [2] address these challenges by enabling p-type conductivity without chemical dopants, achieving room-temperature mobilities up to 32 cm²/Vs [3]. Capping this structure with p-InGaN has previously enabled contact resistance as low as 4.6 Ωmm and pFET on-current above 100 mA/mm, albeit with a Schottky gate and high gate leakage [4]. Here, we demonstrate a GaN pFET with Rc=2.5 Ωmm, low on-resistance, and low gate leakage, enabling on/off ratios above 104 and near E-mode operation.

for V_{ds} = -5 V. Gate leakage is low (<10⁻⁷ mA/mm) for a |V_{gs}|<5V.

C-V analysis of MOS-CAP structures fabricated on the recess-etched GaN surface reveal significant hysteresis (ΔV_T~2V). Drift mobility analysis from integration of the C-V characteristics and TLM-like fitting of the pFET on-resistances vs gate length gives a channel drift mobility that drops from 70 to 10 cm²/Vs for between 10-12 and 10-13 cm⁻² sheet hole density.

Summary of Research:

A p-InGaN/GaN/AlN heterostructure was grown by molecular beam epitaxy on a 2-inch single-crystal AlN substrate. Contactless sheet-resistance mapping showed a uniform sheet resistance of $3.9 \pm 0.3 \text{ k}\Omega/\square$, with sheet hole densities and mobilities of $6.0\text{--}6.6 \times 10^{13} \text{ cm}^{-2}$ and 29 cm²/Vs, respectively, measured on diced pieces before fabrication. Ni/Au contacts alloyed in O₂ exhibit linear I-V characteristics with Rc = $(2.5 \pm 0.4) \text{ }\Omega\text{mm}$. The p-InGaN cap was recess-etched with a low-power (RF = 3 W) chlorine-based ICP-RIE process. A 14 nm AlHfO_x gate dielectric was deposited by thermal ALD and annealed at 300°C for 3 min. All features were defined by optical lithography.

Output characteristics of pFETs with L_g from 1-6 μm exhibit linear turn-on, and approach saturation within V_{gs}=-5V. pFET on-currents scale as 1/L_g, indicating that the devices are in the long-channel regime. Transfer characteristics exhibit near E-mode operation (V_T ~ +1 V), with ~107 on/off ratio for |V_{ds}|<1V and ~104 on/off

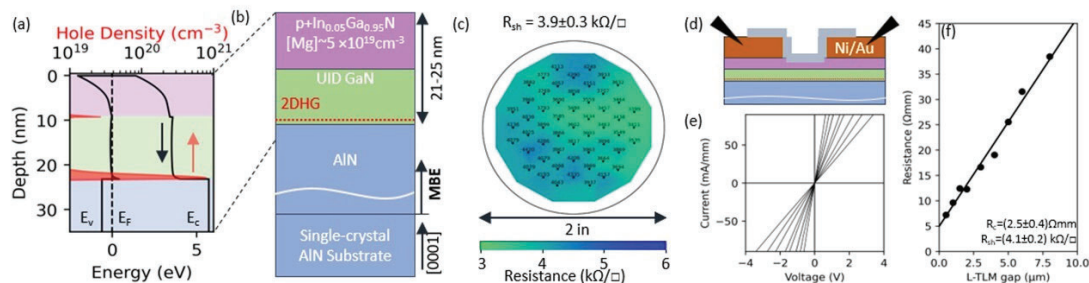


Figure 1: (a-b) p+InGaN/GaN/AlN heterostructure grown by molecular beam epitaxy on a 2'' single-crystal AlN substrate. A polarization-induced two-dimensional hole gas (2DHG) resides at the GaN/AlN interface. (c) Room-temperature transport is highly uniform across the wafer with $R_{sh}=3.9\pm0.3$ kΩ/□. (d-f) Ni/Au ohmic contacts exhibit linear I-V characteristics, with $R_c=(2.5\pm0.4)$ Ωmm.

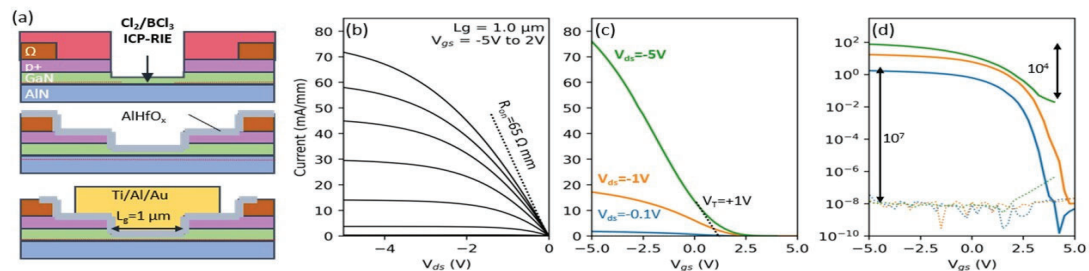


Figure 2: (a) Long-channel ($L_g = 1$ μm) pFET fabricated by Cl₂/BCl₃ ICP-RIE gate-recess etch and atomic layer deposition of a AlHfO_x-based gate dielectric. (b) Output characteristics with $R_{on}(V_{gs}=-5V) = 65$ Ωmm. (c/d) Transfer characteristics on a linear/log scale for $V_{ds} = -0.1, 1.0$, and 5.0 V. The threshold voltage is $V_T = +1$ V; gate leakage is low for $|V_g| < 5$ V, and 7-orders on/off is seen for $|V_d| < 1$ V.

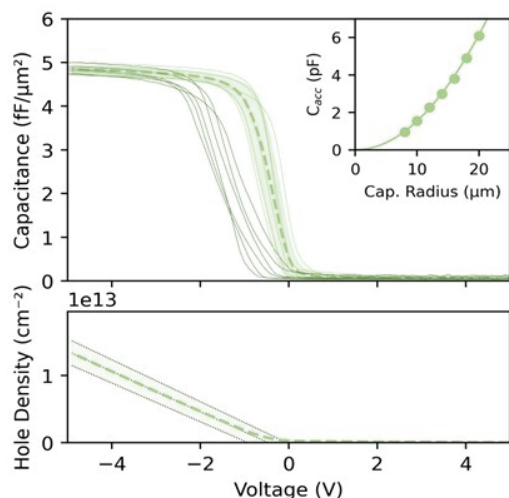


Figure 3: (a) C-V analysis of MOS capacitor structures reveals CCW hysteresis with $\Delta V_{th} \sim 2$ V. (b) The up-sweep integrated hole density exhibits a threshold voltage of $V_T = (-0.5 \pm 0.5)$ V.

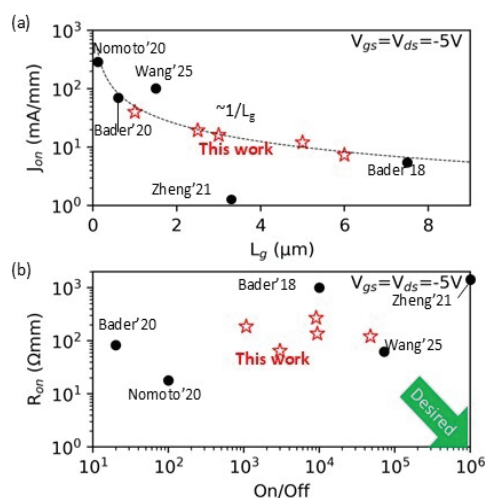


Figure 4: Benchmarking of (a) on-current at $V_{gs} = V_{ds} = -5$ V vs recessed gate length L_g , (b) on-resistance @ $V_{gs} = -5$ V vs on/off ratio for this work, plus select devices in the literature.

Conclusions and Future Steps:

Despite the low contact resistance in these pFETs, the on-currents remain low (<100 mA/mm) due to mobility degradation during the ICP-RIE gate-recess etch, outperformed by pFET designs with thicker GaN channels that protect from recess damage [5]. Future device generations can be improved with lower-damage gate-recess etching and pre-dielectric surface treatments that mitigate hysteresis.

References:

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