

A 16-to-256QAM G-Band Subharmonic Phase-Modulating Transmitter

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Abstract:

Existing analog up-converting transmitters (TX) remain insufficient for achieving desired data rate and spectrum/energy efficiency for beyond-5G (B5G) communications due to their dependence on high-resolution power-hungry DACs and the back-off required by power amplifiers for linearity concerns [1,2]. Prior digital TX designs at sub-THz were limited to low-order modulations, such as OOK [3], BPSK [4], and QPSK [5] due to the dynamic operation range and resolution of existing circuits. While high modulation-order TXs have been demonstrated at E-band [6], it is nontrivial to extend a similar concept to sub-THz frequency regime due to excessive phase-modulator losses [7,8]. Harmonic out-phasing approaches have emerged recently to help alleviate such issues but are constrained to low-order constellations of PSK [9] and STAR-QAM [10] due to the lack of high-speed and fine-resolution phase modulators. To overcome such challenges, a Sub-Harmonic Phase-Modulating Transmitter (SHPM-TX) is presented to achieve high-speed modulations (51.2 Gbps/16QAM, 24 Gbps/64QAM, and 8 Gbps/256QAM) with $-2\text{dBm } P_{\text{OUT}}$ consuming 280-350 mW DC power.

Summary of Research:

Shown in Fig. 1, the SHPM-TX starts by splitting its input at sub-harmonic $f_c/3$ (60–75 GHz) to create dual phasors in parallel with a wideband balun, followed by Digital-to-Time/Phase Converters (DTPC) made of switched-capacitor-controlled differential transmission lines (TL). On-chip SRAM, serializers and Binary-to-Thermometer (B2T) decoders are integrated as high-speed controllers for the DTPC. A subsequent carrier conditioning chain saturates a frequency-tripler, tripling the phase modulation in a time-invariant manner. Symbol synthesis is attained by summing dual constant-envelope phasor voltages through a wideband transformer. The implementation of sub-harmonic DTPC at $f_c/3$ reduces required phase modulation range by 3X, preserves switched-capacitor's quality factor,

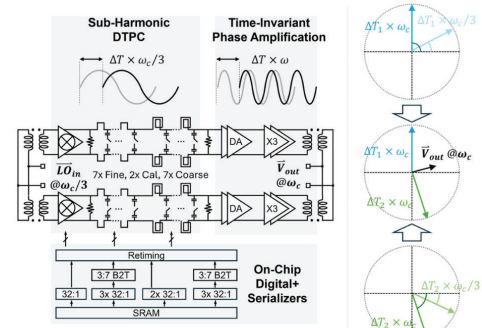


Figure 1: Chip block diagram and operating principles.

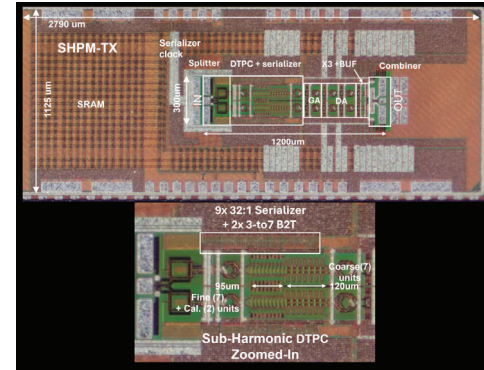


Figure 2: Measured constellations and IF spectrum at 16, 64, 256 QAM at various symbol rates.

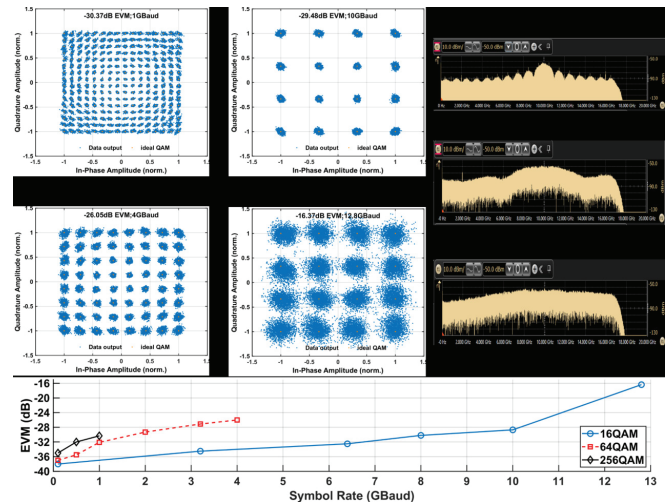


Figure 3: Die photo.

and lowers traveling-wave loss and propagation delay. The switched-capacitor TL, similar to DiCAD [11], delivers finer phase resolution with a smaller footprint than the reflection-type phase shifters [12].

Fig. 2 shows the die photo of a prototype SHPM-TX. The measured EVM versus symbol rate trend is plotted in Fig. 3. The measured EVM's for 1 GBaud/256QAM, 4 GBaud/64QAM, 10 GBaud/16QAM, and 12.8 GBaud/16QAM are -30.37 dB, -26.05 dB, -29.48 dB and -16.37 dB, respectively. Corresponding data rates are 8 Gbps/256QAM, 24 Gbps/64QAM, 40 Gbps/16QAM, and 51.2 Gbps/16QAM. A table to benchmark this work versus prior state-of-the-art sub-THz transmitters and phase shifters is given in Fig. 4. With fully integrated digital baseband and carrier conditioning circuitry in 28 nm CMOS, the SHPM-TX operates from 195-225 GHz, achieving a peak P_{OUT} of -6 to -2 dBm. It features fine phase granularity (down to 0.7° steps and <0.2° rms error) and realizes up to 51.2 Gbps (16QAM), 24 Gbps (64QAM) and 8 Gbps (256QAM), while consuming DC power of 280–350 mW and occupying a 0.36 mm² silicon area. Compared with prior transmitters at 200 GHz and beyond, the SHPM-TX achieves scalable high-order QAM transmissions at higher data rates in a more integrated design.

	This work	ASSCC 22 [9]	JSSC 20 [10]	JSSC 22 [5]	TMTT 23[4]	ISSCC 24 [2]	ISSCC 25 [7]
Technology	28nm CMOS	22nm SOI	28nm CMOS	55nm SiGe	130nm SiGe	65nm CMOS	55nm SiGe
Frequency (GHz)	195-225	110	390	225	245	236-266	125-170
Architecture	Sub-Harmonic Phase-Modulating Transmitter	Harmonic Outphasing Transmitter	Harmonic Outphasing Transmitter	Amplitude Modulation Transmitter	Phase Modulation Transmitter	Analog Up-converter for Phased Array	Outphasing Phase Shifter
Modulator Type	Digital Switched-Capacitor Transmission Line	Analog RTPS	Digital Switched-Capacitor Delay Line	Digital Base-Band Switch	Digital Mixer	N/A	Digital Switched-Capacitor Transmission Line
Digital Control Bits	2 × 16	N/A	2 × 36	1	1	N/A	2 × 48
RMS Phase Shift Step (°)	23.35 (simul.) 3.10 (meas.) 5.92 (cal. 1) 6.71 (cal. 8)	N/A	45	N/A	N/A	2.4	9
RMS Phase Shift Error (°)	2.25 (simul.) 6.35 (meas.) 6.14 (cal. 50) 6.17 (cal. 50)	N/A	N/A	N/A	N/A	N/A	5
Data Rate (Gbps) and Modulation	51.2@16QAM 24@64QAM 8@256QAM	16@QPSK 13.1@BPSK	6@QPSK 16@16QAM 16@64QAM	26@OOK	52@BPSK	10@16QAM 9@64QAM	N/A
(EVM) _{RMS}	-30.37@256QAM -26.05@64QAM -29.48@16QAM	-13.5@QPSK -14.3@BPSK	-11.8@QPSK -16.3@16QAM -16.3@64QAM	N/A	N/A	-19.6@16QAM -16.5@64QAM	N/A
Peak P _{OUT} (dBm)	-6 to -2	16.2	-16	-3*	3.5	-3.4	2 to 3.5
Power Dissipation (mW)	280@1.2G/5A 350@12.8G/5A	334	1100	165.2	414	209**	31
Core Area (mm ²)	0.36	0.54	2	0.89	1.16	2.47	0.2

* Simulated ** On-chip AWG *** Small-signal power

Figure 4: Comparison table against the state-of-the-arts.

Conclusions and Future Steps:

Moving forward, this design is being modified to be packaged with CNF's GaN process in order to demonstrate a TX with state-of-the-art P_{OUT} while preserving the high modulation for future wireless and wireline applications.

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