

Progress of Microscale Flow Sensors

CNF Project Number: 2121-12

Principal Investigator(s): Alyssa Apse

User(s): Yushuang Liu

Affiliation(s): Electrical and Computer Engineering Department, Cornell University

Primary Source(s) of Research Funding: National Science Foundation

Contact: aba25@cornell.edu, yl3835@cornell.edu

Primary CNF Tools Used: ABM, AJA Sputter 1, AJA Sputter 2, Odd-Hour Evaporator, HDP-CVD, Oxford 81, TPT HB16

Abstract:

Pd-based microfluidic sensors have been developed for higher resolution sensing in low Reynolds liquids using CNF tools. The addition of magnetic strips allows force sensing abilities to be characterized. The flow sensing abilities will be tested using a three-electrode cell and a syringe pump.

Summary of Research:

CNF facilities have been utilized greatly during the past year to fabricate palladium (Pd) -based actuators for microfluidic sensing. Previous research has shown that the hydrogen evolution reaction of Pd is affected by strain[1], making it possible to imply the strain, and therefore the flow speed, by tracking the current observed at the Pd-based actuator. We adopt a bilayer cantilever structure with a rigid panel at its top to increase the strain experienced by the actuator. Tools for fabrication include and are not limited to ABM, AJA Sputter, Odd-Hour Evaporator, HDP-CVD, and Oxford 81.

A three-electrode cell is built to test the electrochemistry properties of the actuators. The cell includes a Ag/AgCl reference electrode, a gold counter electrode, and the actuators serve as working electrodes. To demonstrate that the actuators are able to sense forces beyond microfluidics, their force sensing capabilities are tested by adding magnetic strips on the panel, which respond to an external magnetic field generated by Helmholtz coils. The direction and magnitude of the magnetic dipole within the magnetic strips will be mapped out using Atomic Force Microscope (AFM) in CNF.

Conclusions and Future Steps:

Initial test results showed current responses matching expectations. More rigorous experiments will be performed to relate current responses to force and flow speed. The actuators' response to fluidics will be observed in a microfluidic chamber connected to a syringe pump.

References:

- [1] Jansonius, et al. Strain influences the Hydrogen Evolution Activity and Absorption Capacity of Palladium. *Angew. Chem. Int. Ed.* 2020, 59, 12192. <https://doi.org/10.1002/anie.202005248>.

A Scalable Ultra-Low Power Temperature Gradient Sensor using Pulse Coupled Oscillators

CNF Project Number: 2121-12

Principal Investigator(s): Alyssa Apsel

User(s): Kyubum Shim, Parag Chaudhari

Affiliation(s): Electrical and Computer Engineering Department, Cornell University

Primary Source(s) of Research Funding: National Science Foundation

Contact: aba25@cornell.edu, ks975@cornell.edu, prc79@cornell.edu

Primary CNF Tools Used: Wire bonder

Abstract:

This paper presents an ultra-low power and area-efficient temperature sensor array, capable of local temperature measurements and innate gradient detection using locally coupling oscillators. This all-CMOS system consumes approximately $5pW$, occupies $0.0045mm^2$, operates on a wide supply voltage range of 0.6V to 1.8V, and reduces computational overhead for gradient detection within scalable systems.

Summary of Research:

Temperature sensing nodes with distributed inference mechanism to detect local temperature maxima.

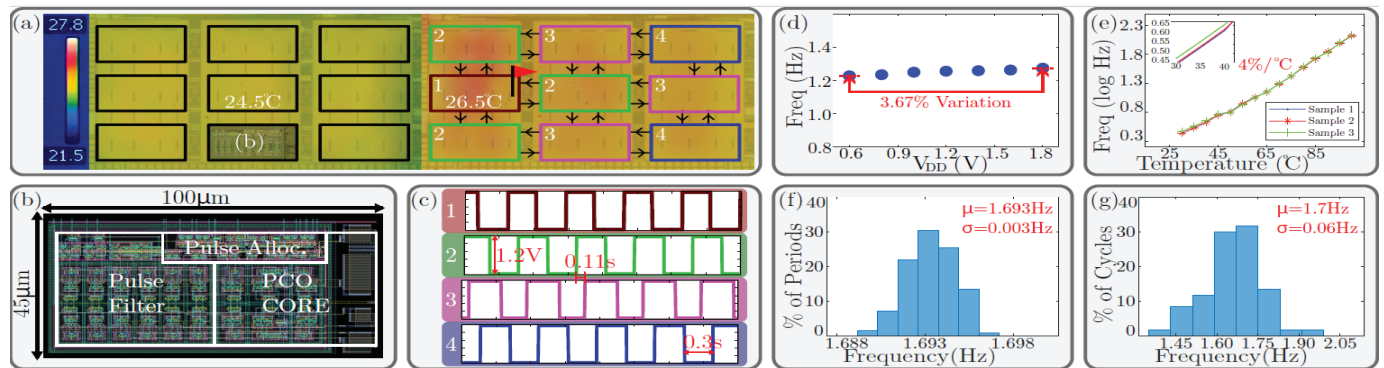


Figure 1.

P-channel GaN Transistors on the AlN Platform

CNF Project Number: 2800-19

Principal Investigator(s): Huili Grace Xing

User(s): Joseph Dill

Affiliation(s): Applied & Engineering Physics, Cornell University

Primary Source(s) of Research Funding: Semiconductor Research Corporation

Contact: grace.xing@cornell.edu, jed296@cornell.edu

Research Group Website: <https://jena-xing.engineering.cornell.edu/>

Primary CNF Tools Used: Heidelberg MLA 150, PT 770, Angstrom E-beam Evaporator, Odd-Hour Evaporator, Oxford FlexAL, Takachi ALE, AJA Ion Mill

Abstract:

The development of complementary GaN electronics requires high-performance p-channel field-effect transistors (pFETs) capable of matching the on-currents of GaN HEMTs [1]. However, p-GaN devices suffer from low hole mobility and poor dopant activation, resulting in high on-resistance and limited output current. Polarization-engineered GaN/AlN heterostructures [2] address these challenges by enabling p-type conductivity without chemical dopants, achieving room-temperature mobilities up to $32 \text{ cm}^2/\text{Vs}$ [3]. Capping this structure with p-InGaN has previously enabled contact resistance as low as $4.6 \text{ } \Omega\text{mm}$ and pFET on-current above 100 mA/mm , albeit with a Schottky gate and high gate leakage [4]. Here, we demonstrate a GaN pFET with $R_c=2.5 \text{ } \Omega\text{mm}$, low on-resistance, and low gate leakage, enabling on/off ratios above 104 and near E-mode operation.

for $V_{ds} = -5 \text{ V}$. Gate leakage is low ($<10^{-7} \text{ mA/mm}$) for a $|V_{gs}| < 5 \text{ V}$.

C-V analysis of MOS-CAP structures fabricated on the recess-etched GaN surface reveal significant hysteresis ($\Delta V_T \sim 2 \text{ V}$). Drift mobility analysis from integration of the C-V characteristics and TLM-like fitting of the pFET on-resistances vs gate length gives a channel drift mobility that drops from 70 to $10 \text{ cm}^2/\text{Vs}$ for between 10^{-12} and 10^{-13} cm^{-2} sheet hole density.

Summary of Research:

A p-InGaN/GaN/AlN heterostructure was grown by molecular beam epitaxy on a 2-inch single-crystal AlN substrate. Contactless sheet-resistance mapping showed a uniform sheet resistance of $3.9 \pm 0.3 \text{ k}\Omega/\square$, with sheet hole densities and mobilities of $6.0\text{--}6.6 \times 10^{13} \text{ cm}^{-2}$ and $29 \text{ cm}^2/\text{Vs}$, respectively, measured on diced pieces before fabrication. Ni/Au contacts alloyed in O_2 exhibit linear I-V characteristics with $R_c = (2.5 \pm 0.4) \text{ } \Omega\text{mm}$. The p-InGaN cap was recess-etched with a low-power ($\text{RF} = 3 \text{ W}$) chlorine-based ICP-RIE process. A 14 nm AlHfOx gate dielectric was deposited by thermal ALD and annealed at 300°C for 3 min. All features were defined by optical lithography.

Output characteristics of pFETs with L_g from $1\text{--}6 \text{ } \mu\text{m}$ exhibit linear turn-on, and approach saturation within $V_{gs} = -5 \text{ V}$. pFET on-currents scale as $1/L_g$, indicating that the devices are in the long-channel regime. Transfer characteristics exhibit near E-mode operation ($V_T \sim +1 \text{ V}$), with ~ 107 on/off ratio for $|V_{ds}| < 1 \text{ V}$ and ~ 104 on/off

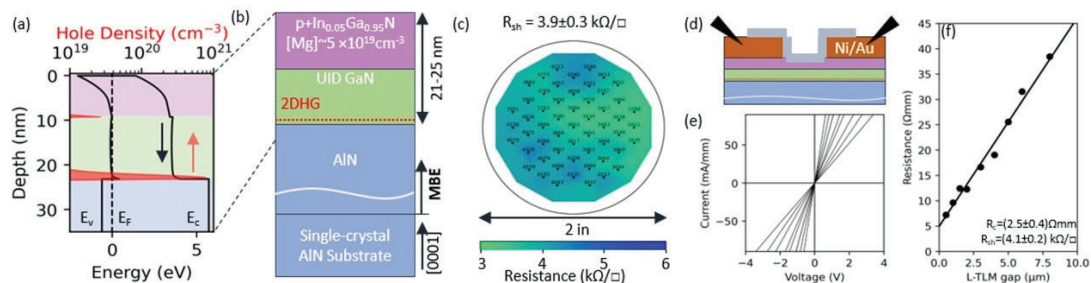


Figure 1: (a-b) p-InGaN/GaN/AlN heterostructure grown by molecular beam epitaxy on a 2'' single-crystal AlN substrate. A polarization-induced two-dimensional hole gas (2DHG) resides at the GaN/AlN interface. (c) Room-temperature transport is highly uniform across the wafer with $R_{sh}=3.9\pm0.3$ kΩ/□. (d-f) Ni/Au ohmic contacts exhibit linear I-V characteristics, with $R_c=(2.5\pm0.4)$ Ωmm.

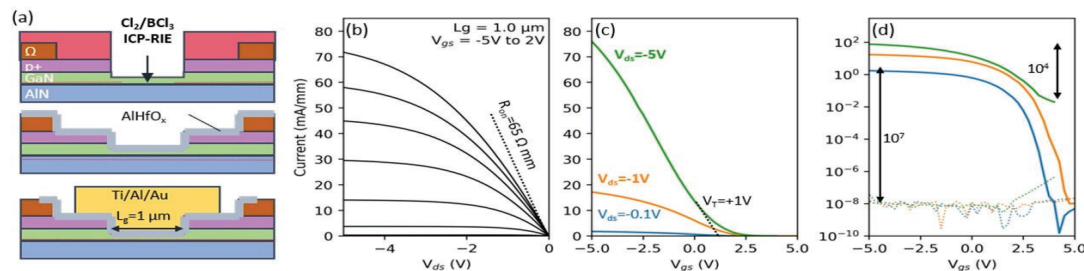


Figure 2: (a) Long-channel ($L_g = 1$ μm) pFET fabricated by Cl₂/BCl₃ ICP-RIE gate-recess etch and atomic layer deposition of a AlHfO_x-based gate dielectric. (b) Output characteristics with $R_{on}(V_{gs}=-5V) = 65$ Ωmm. (c/d) Transfer characteristics on a linear/log scale for $V_{ds} = -0.1, 1.0$, and 5.0 V. The threshold voltage is $V_T = +1$ V; gate leakage is low for $|V_g| < 5$ V, and 7-orders on/off is seen for $|V_d| < 1$ V.

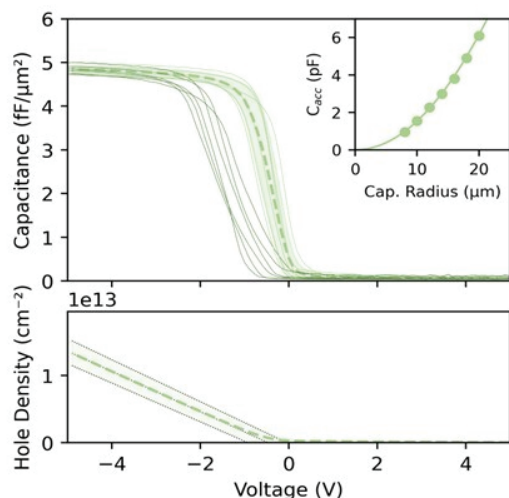


Figure 3: (a) C-V analysis of MOS capacitor structures reveals CCW hysteresis with $\Delta V_{th} \sim 2$ V. (b) The up-sweep integrated hole density exhibits a threshold voltage of $V_T = (-0.5 \pm 0.5)$ V.

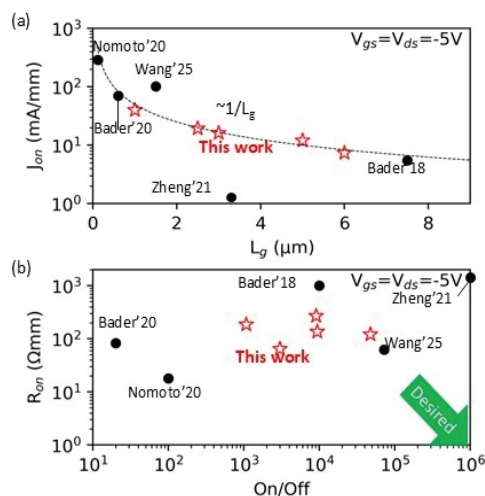


Figure 4: Benchmarking of (a) on-current at $V_{gs} = V_{ds} = -5$ V vs recessed gate length L_g , (b) on-resistance @ $V_{gs} = -5$ V vs on/off ratio for this work, plus select devices in the literature.

Conclusions and Future Steps:

Despite the low contact resistance in these pFETs, the on-currents remain low (<100 mA/mm) due to mobility degradation during the ICP-RIE gate-recess etch, outperformed by pFET designs with thicker GaN channels that protect from recess damage [5]. Future device generations can be improved with lower-damage gate-recess etching and pre-dielectric surface treatments that mitigate hysteresis.

References:

- [1] Bader, Samuel James, et al. IEEE Trans. on Elec. Dev. 67.10 (2020): 4010-4020.
- [2] Reet Chaudhuri et al., Science 365,1454-1457 (2019).
- [3] C. F. C. Chang, et al., Nat. Electron. 9, 346–357 (2026).
- [4] S. J. Bader et al., IEDM, San Francisco, CA, USA, 2019, pp. 4.5.1-4.5.4.
- [5] Z. Wang, Appl. Phys. Lett. 126, 152104 (2025).

Applications of SF₆/Cl₂/BCl₃ ALE for III-Nitrides

CNF Project Number: 2800-19

Principal Investigator(s): Huili Grace Xing

User(s): Rafail Panagiotopoulos

Affiliation(s): Department of Materials Science and Engineering

Primary Source(s) of Research Funding: SUPREME

Contact: grace.xing@cornell.edu, rp638@cornell.edu

Research Group Website: <https://jena-xing.engineering.cornell.edu/>

Primary CNF Tools Used: Takachi ALE, FlexAL ALD, Odd hour evaporator, MLA maskless lithography

Abstract:

This study demonstrates the successful atomic layer etching of aluminum nitride and gallium nitride using sequential exposures to SF₆ plasma for surface fluorination, followed by Cl₂/BCl₃ plasma to remove the altered layer at or below 100 °C. We investigated the applications of this ALE recipe in achieving improved ohmic contacts to highly doped 71% n-AlGaIn, especially when compared to other plasma based etching techniques. Several techniques were performed, including AFM, XPS, in-situ ellipsometry and probe station measurements for TLM analysis.

Summary of Research:

Gallium nitride (GaN) and aluminum nitride (AlN), both belonging to the III–V semiconductor group, play a pivotal role in modern electronic and photonic technologies. Their wide bandgaps, strong thermal stability, and intrinsic piezoelectric properties make them particularly suitable for fabricating high electron mobility transistors (HEMTs), which are commonly used in radio-frequency (RF) and power electronics applications^{1–3}. Additionally, due to their outstanding optical characteristics, GaN and AlN are also emerging as key materials for photonic integrated circuits and light-emitting diodes (LEDs)^{4,5}.

Atomic Layer Etching (ALE) operates on the principle of dividing the etching process into a series of self-limiting, sequential steps. This separation allows for precise control over the formation and transport of reactive species, enabling improved process uniformity and avoiding the surface damage typically associated with reactive ion etching. The ALE cycle generally comprises two distinct phases: a surface modification step that lowers the material's surface binding energy, followed by a removal step^{6,7}.

Utilizing SF₆ plasma for surface modification and Cl₂/BCl₃ plasma for removal, we achieved etch rates of 4.47 Å/cycle and 5.92 Å/cycle for AlN and GaN respectively,

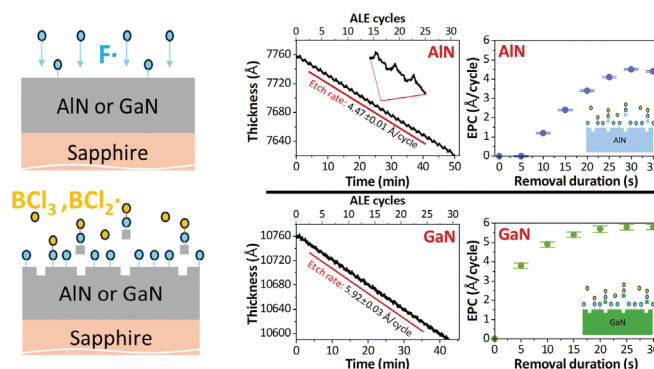


Figure 1: Etch rates and saturation behavior for AlN and GaN.

which correspond approximately to one unit cell per cycle. Etch rate was monitored with in-situ ellipsometry as seen in Figure 1. This approach displayed very controlled results, achieving ALE at temperatures significantly lower than thermal ALE, down to even 40°C (Figure 2). Furthermore, this technique was used to treat n-AlGaIn surfaces prior to ohmic contact metallization. The Si doped AlGaIn samples were grown on single crystal AlN substrate by plasma-assisted molecular beam epitaxy (MBE) with a Si density of $9 \times 10^{19} \text{ cm}^{-3}$. 10 nm of n+AlGaIn were etched on 3 samples with ALE, high etch rate Cl₂/BCl₃/Ar ICP-RIE and low etch rate BCl₃ ICP-RIE. Ti/Al/Ti contacts were deposited by e-beam evaporation and annealed at 900°C for 30 s in N₂ atmosphere. ALE leads to increased linearity in the I–V characteristics of the contacts. Current dependent TLM analysis showed that ALE led to the lowest contact resistivity and highest uniformity with $\rho_c = (2.50 \pm 0.14) \times 10^{-4} \Omega \text{ cm}^2$ at 0 A (Figure 3). Atomic Force Microscopy (AFM) was utilized to study the effect of etching on surface morphology (Figure 4). These results render ALE a great alternative to conventional ICP-RIE to improve performance in high Al composition AlGaIn devices.

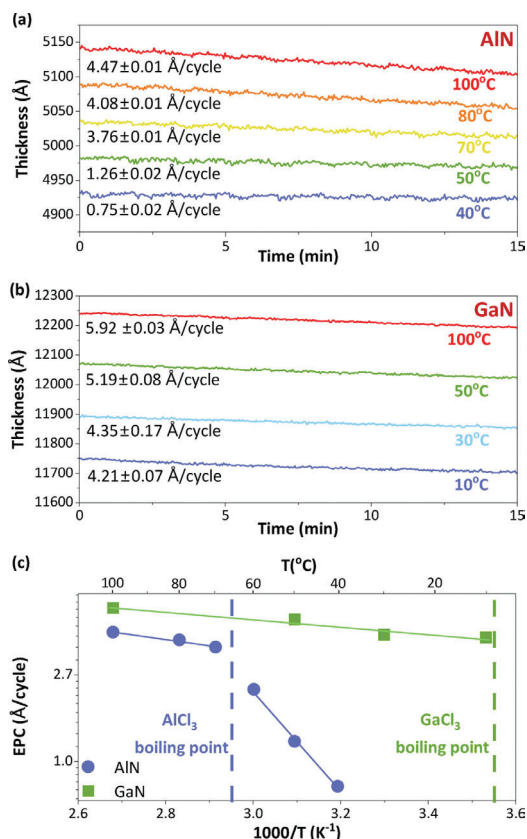


Figure 2: Temperature dependence of ALE.

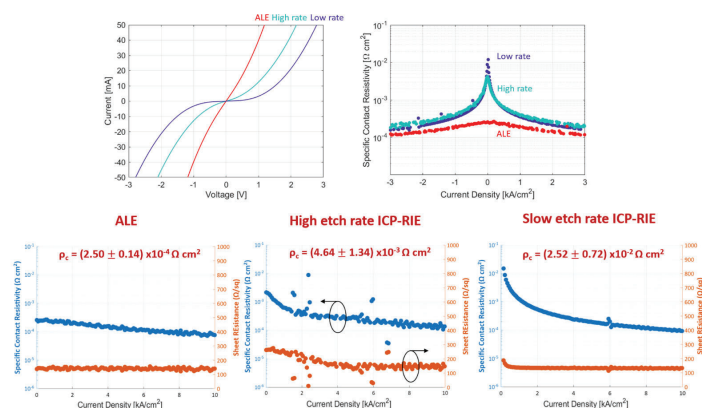


Figure 3: I-V characteristics of ohmic contacts and current dependent linear TLM analysis

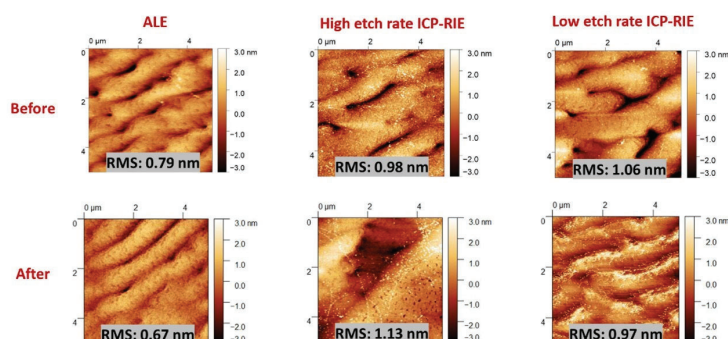


Figure 4: 5 x 5 μm² AFM scans of n+AlGaIn surface before and after etching.

References:

- [1] U. Mishra, P. Parikh, and Y.-F. Wu, "Algan/gan hemts—an overview of device operation and applications," *Proceedings of the IEEE* 90, 1022–1031 (2002).
- [2] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial gan power devices and gan-based converter design challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics* 4, 707–719 (2016).
- [3] A. L. Hickman, R. Chaudhuri, S. J. Bader, K. Nomoto, L. Li, J. C. M. Hwang, H. Grace Xing, and D. Jena, "Next generation electronics on the ultrawide-bandgap aluminum nitride platform," *Semiconductor Science and Technology* 36, 044001 (2021).
- [4] S. Nakamura and M. R. Krames, "History of gallium–nitride-based light-emitting diodes for illumination," *Proceedings of the IEEE* 101, 2211–2220 (2013).
- [5] C. Xiong, W. H. P. Pernice, X. Sun, C. Schuck, K. Y. Fong, and H. X. Tang, "Aluminum nitride as a new material for chip-scale optomechanics and nonlinear optics," *New Journal of Physics* 14 (2012).
- [6] K. J. Kanarik, S. Tan, and R. A. Gottscho, "Atomic layer etching: Rethinking the art of etch," *The Journal of Physical Chemistry Letters* 9, 4814–4821 (2018).
- [7] K. J. Kanarik, T. Lill, E. A. Hudson, S. Sriraman, S. Tan, J. Marks, V. Vahedi, and R. A. Gottscho, "Overview of atomic layer etching in the semiconductor industry," *Journal of Vacuum Science Technology A* 33, 020802 (2015).

SiN Passivated AlScN-Barrier HEMTs Demonstrating Negligible Current Dispersion

CNF Project Number: 2800-19

Principal Investigator(s): Huili Grace Xing

User(s): Hanqiao Zhang

Affiliation(s): School of Electrical and Computer Engineering, Department of Materials Science and Engineering

Contact: grace.xing@cornell.edu, hz587@cornell.edu

Primary CNF Tools Used: PECVD, PT770, GaN LPCVD, e-beam evaporator, JEOL-6300, MLA150

Abstract:

Aluminum scandium nitride (AlScN) has emerged as a promising barrier and dielectric material for gallium nitride (GaN) high-electron-mobility transistors (HEMTs) due to its large spontaneous polarization, high dielectric constant, and the strain balance with GaN [1]. In addition, the high-k nature of AlScN allows thicker effective barrier layers that reduce gate leakage without sacrificing gate capacitance, providing a pathway toward simultaneous improvements in breakdown voltage and radio-frequency (RF) performance. In AlScN/GaN heterostructures, high drain current and speed have been demonstrated [1], [2]. In this work, we report significant suppression of current dispersion in AlScN HEMTs through low-pressure chemical-vapor-deposition (LPCVD) silicon nitride (SiN) passivation, an essential step towards building the next generation AlScN based RF electronics.

Summary of Research:

The AlScN/GaN heterostructure in this work was grown by plasma-assisted molecular beam epitaxy (MBE). As shown in Fig. 1, it consists of a GaN/Al_{0.84}Sc_{0.16}N/GaN/AlN top barrier on 830-nm GaN with AlN buffer grown on a semi-insulating 4H-SiC substrate. The energy band diagram of the full heterostructure is shown. Device fabrication started with definition of the source/drain regions using a SiO₂/Cr hard mask. After ICP etching through the barrier into the UID GaN using the hard mask, n+ GaN regrowth by MBE was performed. After removal

of masked regions, mesa isolation was performed, and ~74-nm of near stoichiometric Si₃N₄ was deposited using LPCVD. A non-alloyed Ti/Au source/drain metal stacks were deposited through e-beam evaporation. Lastly, a gate-recess etch was performed via low-power timed SF₆ ICP etch, and gates were metallized by e-beam evaporation of Ni/Au = 40/350 nm. Following the MBE growth, Hall-effect measurements were performed at room temperature using soldered indium contacts to the 2-dimensional electron gas. The measurement reveals an electron mobility of 1180 cm²/V·s, 2DEG sheet density $n_s \sim 2.38 \times 10^{13}$ /cm², and $R_{sh} = 337 \Omega/\text{sq}$. DC transfer measurements were performed on a device with $L_G = 1 \mu\text{m}$ and $L_{SD} = 5 \mu\text{m}$. As shown in Fig. 2, at a fixed $V_{DS} = 5 \text{ V}$, a peak extrinsic transconductance of 0.42 S/mm was measured. The device exhibited negligible hysteresis and an extrapolated threshold voltage of -3.0 V. An on/off ratio of greater than 10^5 was measured, revealing excellent gate control. Fig. 3 shows the three-terminal off-state breakdown characteristics of the devices with varying L_{GD} . The breakdown was limited by gate-leakage current, far from the intrinsic material limits [2]. Fig. 4 reveals the three-terminal output characteristics of the device. A peak drain current of 1.7 A/mm was measured at $V_{GS} = 2 \text{ V}$. Pulsed I-V measurements were performed on the HEMT device with LPCVD SiN passivation using 500 ns long pulses with a 1 ms period. The sample exhibited negligible current collapse of less than 5% under bias conditions of $V_{GS,q} = -5 \text{ V}$, $V_{DS,q} = 0 \text{ V}$, and $V_{GS,q} = -5 \text{ V}$, $V_{DS,q} = 40 \text{ V}$.

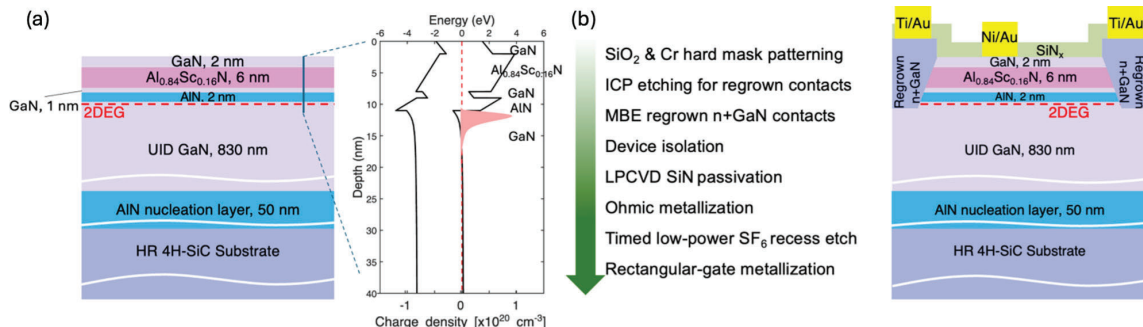


Figure 1:(a) cross-sectional representation of the GaN/Al_{0.84}Sc_{0.16}N/GaN/AlN heterostructure on SiC substrate and the energy band diagram evaluated by self-consistently solving Schrodinger and Poisson equations. (b) device process flow of AlScN/GaN HEMTs.

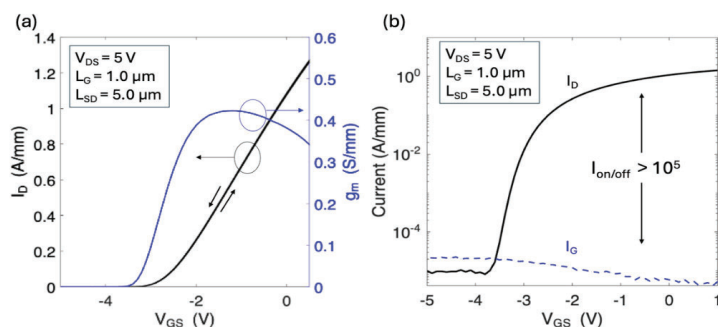


Figure 2: (a) Transfer characteristics of a HEMT device in linear scale, and peak extrinsic transconductance of 0.42 S/mm. (b) Transfer curve in semi-log scale with gate leakage current shown in dotted blue line, demonstrating an on/off ratio greater than 10^5 .

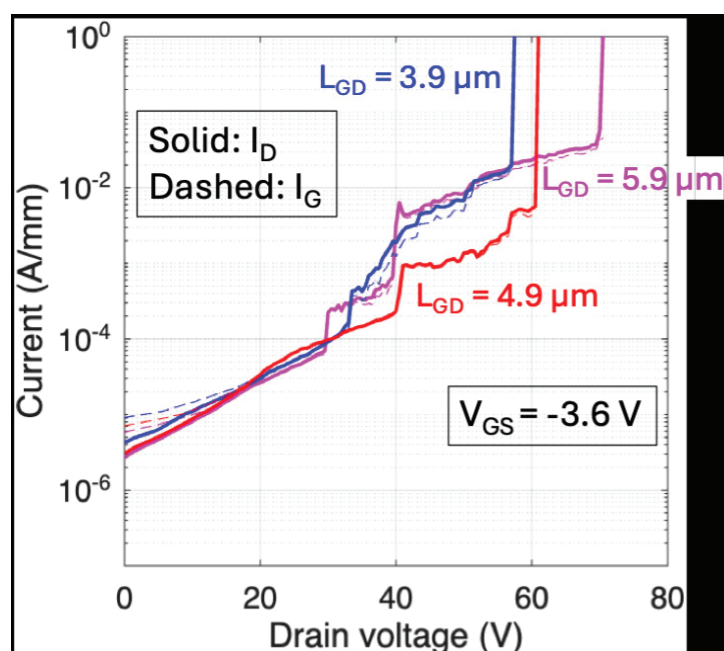


Figure 3: The three terminal off-state breakdown measurements with different gate-drain distance.

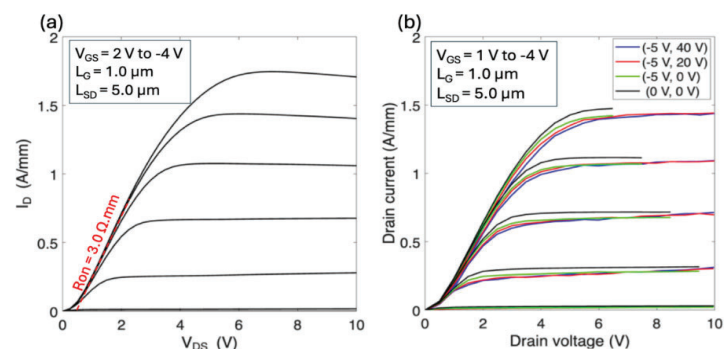


Figure 4: (a) I-V output characteristics of the HEMT device demonstrating a maximum drain current density of 1.7 A/mm. (b) pulsed output measurements of a HEMT device with LPCVD SiN surface passivation demonstrating negligible current dispersion.

Conclusions and Future Steps:

The fabricated AlScN/GaN HEMT is well-suited for RF amplifications due to effectively suppressing current dispersion through LPCVD SiN deposition.

References:

- [1] T. S. Nguyen et al., IEDM, pp. 1–4 (2024).
- [2] K. Nomoto et al., Appl. Phys. Express 18, 016506 (2025).
- [3] E. M. Chumbes et al., IEEE MTT-S IMS, pp. 295–297 (2022).
- [4] A. J. Green et al., IEEE Electron Device Lett. 41, 1181 (2020).
- [5] S. Krause et al., IEEE Electron Device Lett. 44, 17 (2023).
- [6] M. B. Tahhan et al., IEEE Trans. Electron Devices 69, 962 (2022).

SUPREME Tasks 6/7

CNF Project Number: 3078-23

Principal Investigator(s): James Hwang

User(s): Yunjiang Ding, Jin Hong Joo

Affiliation(s): Department of Materials Science and Engineering, Cornell University

Primary Source(s) of Research Funding: SRC/DARPA

Contact: jch263@cornell.edu, yd439@cornell.edu, jj593@cornell.edu

Primary CNF Tools Used: SUSS MA6-BA6 Contact Aligner, Unaxis 770 Deep Silicon Etcher, AJA Ion Mill, AJA Sputter Deposition, Veeco Savannah ALD, Electroplating Hood – Au/Cu, P7 Profilometer, Zygo Optical Profilometer, Pico MA FinePlacer FlipChip Bonder, HFTL DC Probe Station, HFTL Small-Signal Probe Station, HFTL Terahertz Small-Signal Probe Station, PlasmaTherm Singulator, Logitech Orbis CMP

Abstract:

As the demand for heterogeneous integration for RF chiplets continues to grow, through-substrate vias (TSVs) with low loss at millimeter-wave frequencies have become increasingly important. In this study, we investigate TSVs through 200- μm -thick Si interposers. The Si wafers are first thinned and patterned, followed by TSV formation using the Bosch deep reactive ion etching (DRIE) process. The TSV sidewalls are subsequently metallized with Pt by atomic layer deposition (ALD) and filled with electroplated Cu. To enable heterogeneous integration, fine-pitch Cu pillars are fabricated and electrically characterized. Cu pillars approximately 50 μm in diameter and 13- μm high, exhibit a DC series resistance below 1 Ω . Separately, to demonstrate millimeter-wave heterogeneous integration, a GaN-on-Si chiplet with Cu pillars is thermocompression-bonded onto a SiC interposer with Au contacts. The resulting Cu-Au interconnects exhibit a series resistance below 1 Ω , confirming the viability of the proposed interconnect technology for heterogeneous integration of millimeter-wave circuits.

Summary of Research:

To demonstrate Si interposer fabrication and to establish a robust process flow, we use thinned 150-mm high-resistivity (HR) Si wafers with a thickness of approximately 200 μm and a resistivity greater than 5 $\text{k}\Omega\cdot\text{cm}$. Each Si wafer is initially thinned using the PT Singulator. Once the DISCO grinder becomes available, this thinning step will be transitioned to the DISCO system to achieve smoother surface. 50-nm-thick Al_2O_3 is subsequently deposited on the backside of the wafer using the AJA sputter deposition system. Al_2O_3 was selected as hard mask because of its 1000:1 selectivity during the Bosch DRIE process of alternating C_4F_8 and SF_6 gases. Currently, TSVs are fabricated using the UNAXIS 770 Deep Silicon Etcher. As the fabrication

process matures, this step will be transition to the PlasmaTherm Singulator platform.

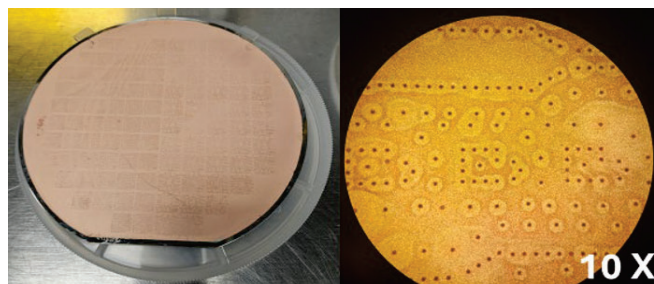


Figure 1: (a) Micrograph of Cu-plated 150-mm HR Si wafer and (b) detailed view of TSVs.

After the TSVs are completely etched, ALD is used to conformally deposit a Pt seed layer on the TSV sidewalls. Cu is then electroplated to fill the TSVs (Fig. 1). Following the backside processing, the front side of the wafer is patterned into Ti/Al transmission lines using the AJA sputter deposition system. The fabrication sequence and completed Si interposer structure are shown in Fig. 2.

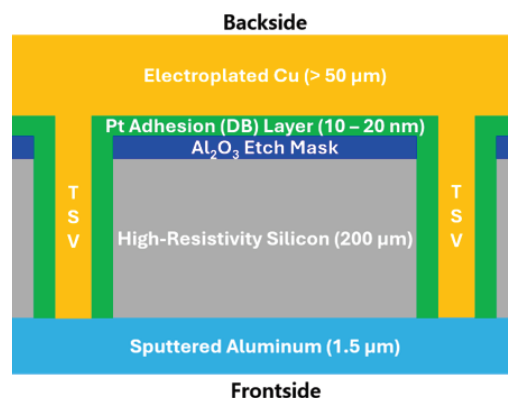


Figure 2: Si interposer cross-section schematic.

Cu pillars are fabricated on a Si substrate using a 200-nm Pt seed layer. A photoresist mold was formed using SPR220 photoresist and an image-reversal process to create an undercut profile. Copper is then electroplated to form cylindrical pillars with diameters of approximately 50 μm and heights of approximately 13 μm (Fig. 3). Electrical characterization shows that the fabricated Cu-pillar interconnects have a series resistance below 1 Ω , demonstrating their suitability for low-resistance, fine-pitch flip-chip integration.

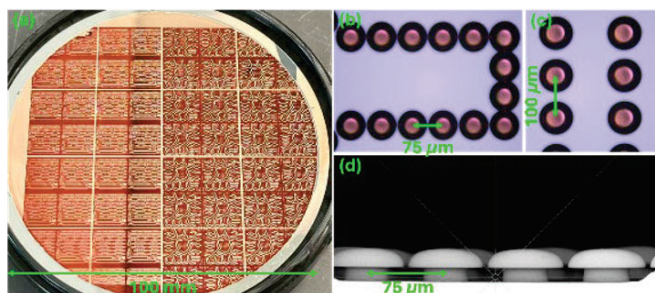


Figure 3: (a) Optical top view of a 100-mm Si wafer electroplated with Cu. (b) Optical top view and SEM side view of Cu pillars.

For RF heterogeneous integration, a GaN-on-Si chiplet is flip-chip bonded onto a SiC interposer through Cu-Au contacts using thermocompression bonding at 350 $^{\circ}\text{C}$ with an applied bonding force of 5 N for 5 min (Fig. 4). The resulting Cu-Au interconnects exhibited a series DC resistance below 1 Ω .

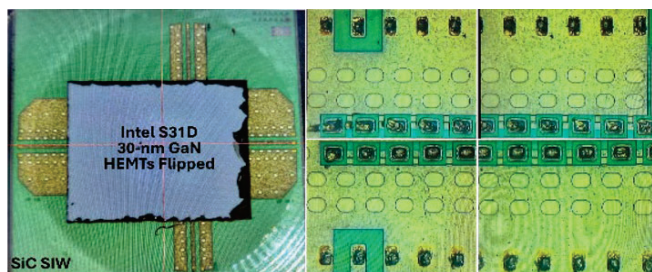


Figure 4: Top-view micrographs of (a) a GaN-on-Si chiplet flip-chip-bonded on a SiC interposer and (b) uniform footprints on the interposer after removal of the chiplet.

Conclusions and Future Steps:

The fabrication of Si interposers focused on optimizing the Bosch DRIE process for thin HR Si wafers and refining the metallization process to achieve uniform anisotropic TSV etching and reliable Cu filling across the wafer. With upgraded fabrication capabilities and an improved design incorporating on-wafer calibration standards, TSV-grounded transmission lines are expected to achieve a new state of the art performance with insertion loss below 0.5 dB/mm up to 140 GHz. Their RF performance will be characterized using HFTL's 220-GHz single-sweep probe station.

The demonstrated low-resistance Cu-pillar interconnects and successful GaN-on-Si flip-chip bonding onto SiC interposers confirm the feasibility of heterogeneous integration for millimeter-wave transceiver frontends. Future work will focus on fabricating finer-pitch Cu pillars on SiC, HR Si, and AlN interposers, followed by comprehensive small-signal millimeter-wave characterization of the flip-chip interconnects and heterogeneously integrated GaN-on-Si chiplet on SiC interposer.

A 16-to-256QAM G-Band Subharmonic Phase-Modulating Transmitter

CNF Project Number: 3096-23

Principal Investigator(s): Mau-Chung Frank Chang

User(s): Christopher Chen, Jia Zhou

Affiliation(s): University of California, Los Angeles (UCLA), Department of Electrical and Computer Engineering

Primary Source(s) of Research Funding: TSMC Joint Development Program

Contact: mfchang@ee.ucla.edu, cchen12@ucla.edu, zhou.jia@ucla.edu

Research Group Website: <https://research.seas.ucla.edu/high-speed-electronics-lab/>

Abstract:

Existing analog up-converting transmitters (TX) remain insufficient for achieving desired data rate and spectrum/energy efficiency for beyond-5G (B5G) communications due to their dependence on high-resolution power-hungry DACs and the back-off required by power amplifiers for linearity concerns [1,2]. Prior digital TX designs at sub-THz were limited to low-order modulations, such as OOK [3], BPSK [4], and QPSK [5] due to the dynamic operation range and resolution of existing circuits. While high modulation-order TXs have been demonstrated at E-band [6], it is nontrivial to extend a similar concept to sub-THz frequency regime due to excessive phase-modulator losses [7,8]. Harmonic out-phasing approaches have emerged recently to help alleviate such issues but are constrained to low-order constellations of PSK [9] and STAR-QAM [10] due to the lack of high-speed and fine-resolution phase modulators. To overcome such challenges, a Sub-Harmonic Phase-Modulating Transmitter (SHPM-TX) is presented to achieve high-speed modulations (51.2 Gbps/16QAM, 24 Gbps/64QAM, and 8 Gbps/256QAM) with $-2\text{dBm } P_{\text{OUT}}$ consuming 280-350 mW DC power.

Summary of Research:

Shown in Fig. 1, the SHPM-TX starts by splitting its input at sub-harmonic $f_c/3$ (60–75 GHz) to create dual phasors in parallel with a wideband balun, followed by Digital-to-Time/Phase Converters (DTPC) made of switched-capacitor-controlled differential transmission lines (TL). On-chip SRAM, serializers and Binary-to-Thermometer (B2T) decoders are integrated as high-speed controllers for the DTPC. A subsequent carrier conditioning chain saturates a frequency-tripler, tripling the phase modulation in a time-invariant manner. Symbol synthesis is attained by summing dual constant-envelope phasor voltages through a wideband transformer. The implementation of sub-harmonic DTPC at $f_c/3$ reduces required phase modulation range by 3X, preserves switched-capacitor's quality factor,

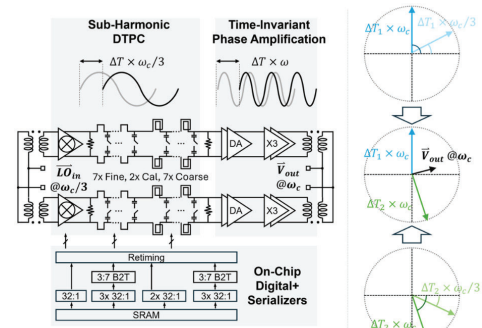


Figure 1: Chip block diagram and operating principles.

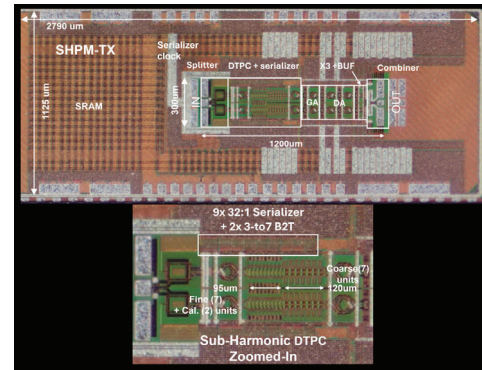


Figure 2: Measured constellations and IF spectrum at 16, 64, 256 QAM at various symbol rates.

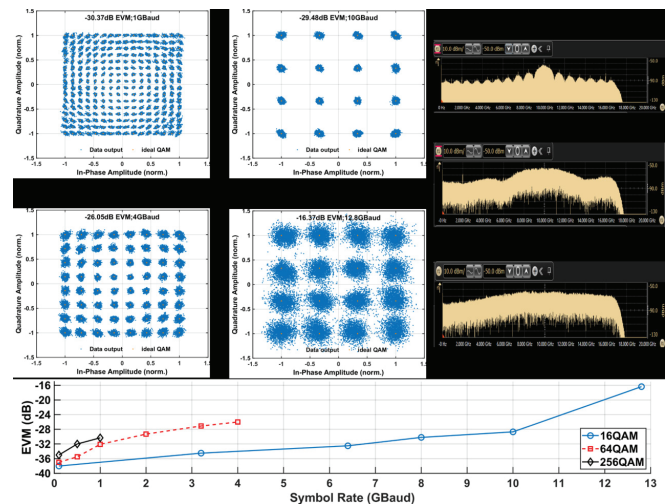


Figure 3: Die photo.

and lowers traveling-wave loss and propagation delay. The switched-capacitor TL, similar to DiCAD [11], delivers finer phase resolution with a smaller footprint than the reflection-type phase shifters [12].

Fig. 2 shows the die photo of a prototype SHPM-TX. The measured EVM versus symbol rate trend is plotted in Fig. 3. The measured EVM's for 1 GBaud/256QAM, 4 GBaud/64QAM, 10 GBaud/16QAM, and 12.8 GBaud/16QAM are -30.37 dB, -26.05 dB, -29.48 dB and -16.37 dB, respectively. Corresponding data rates are 8 Gbps/256QAM, 24 Gbps/64QAM, 40 Gbps/16QAM, and 51.2 Gbps/16QAM. A table to benchmark this work versus prior state-of-the-art sub-THz transmitters and phase shifters is given in Fig. 4. With fully integrated digital baseband and carrier conditioning circuitry in 28 nm CMOS, the SHPM-TX operates from 195-225 GHz, achieving a peak P_{OUT} of -6 to -2 dBm. It features fine phase granularity (down to 0.7° steps and <0.2° rms error) and realizes up to 51.2 Gbps (16QAM), 24 Gbps (64QAM) and 8 Gbps (256QAM), while consuming DC power of 280–350 mW and occupying a 0.36 mm² silicon area. Compared with prior transmitters at 200 GHz and beyond, the SHPM-TX achieves scalable high-order QAM transmissions at higher data rates in a more integrated design.

	This work	ASSCC 22 [9]	JSSC 26 [10]	JSSC 22 [7]	TMT 23[4]	ISSCC 24 [5]	ISSCC 25 [7]
Technology	28nm CMOS	22nm SiC	28nm CMOS	55nm SiGe	130nm SiGe	65nm CMOS	55nm SiGe
Frequency (GHz)	195-225	110	390	225	246	226-266	125-170
Architecture	Sub-Harmonic Phase-Modulating Transmitter	Harmonic Outphasing Transmitter	Harmonic Outphasing Transmitter	Amplitude Modulation Transmitter	Phase Modulation Transmitter	Analog Up-converter for Phased Array	Outphasing Phase Shifter
Modulator Type	Digital Switched-Capacitor Transmission Line	Analog RTPS	Digital Switched-Capacitor Delay Line	Digital Bias On-Off Switch	Digital Mixer	N/A	Digital Switched-Capacitor Transmission Line
Digital Control Bits	2 × 16	N/A	2 × 36	1	1	N/A	2 × 48
RMS Phase Shift Step (°)	23.25(cal.) 3.10(cal.) 0.81(cal. 1) 0.71(cal. 8)	N/A	45	N/A	N/A	2.4	9
RMS Phase Shift Error (°)	2.25(cal.) 0.30(cal.) 0.14(cal. 50) 0.17(cal. 50)	N/A	N/A	N/A	N/A	N/A	5
Data Rate (Gbps) and Modulation	51.2@16QAM 24@64QAM 8@256QAM	16@QPSK	6@QPSK 16@16QAM	26@OOK	52@BPSK	10@16QAM 56@10QAM	N/A
(EVM) _{RMS}	-30.37@16QAM -26.05@64QAM -29.48@16QAM	-13.1@QPSK	-11.6@QPSK -10.3@16QAM	N/A	N/A	-19.6@16QAM -16.5@16QAM	N/A
Peak P _{OUT} (dBm)	-6 to -2	16.2	-16	-3*	3.5	-3.4	2 to 3.5
Power Dissipation(mW)	280@3.2G/5A 350@12.8G/5A	334	1100	165.2	434	209**	31
Core Area(mm ²)	0.36	0.54	2	0.89	1.16	2.47	0.2

* Simulated ** On-chip AWG *** Small-signal power

Figure 4: Comparison table against the state-of-the-arts.

Conclusions and Future Steps:

Moving forward, this design is being modified to be packaged with CNF's GaN process in order to demonstrate a TX with state-of-the-art P_{OUT} while preserving the high modulation for future wireless and wireline applications.

References:

- [1] K. Takano et al., "A 105Gb/s 300GHz CMOS Transmitter," ISSCC, pp. 308-309, Feb. 2017.
- [2] C. Wang et al., "A 236-to-266GHz 4-Element Amplifier-Last Phased-Array Transmitter in 65nm CMOS," ISSCC, pp. 415-417, Feb. 2024.
- [3] B. Hadidian et al., "A 220-GHz Energy-Efficient High-Data-Rate Wireless ASK Transmitter Array," IEEE JSSC, vol. 57, no. 6, pp. 1623-1634, June 2022.
- [4] L. Steinweg et al., "8.0-pJ/bit BPSK Transmitter with LO Phase Steering and 52-Gbps Data Rate Operating at 246 GHz," IEEE TMTT, vol. 71, no. 7, pp. 3217-3226, July 2023.
- [5] S. Kang et al., "A 240 GHz Fully Integrated Wideband QPSK Transmitter in 65 nm CMOS," IEEE JSSC, vol. 50, no. 10, pp. 2256-2267, Oct. 2015.
- [6] J. Zhou et al., "A 71-86GHz 1024QAM Direct-Carrier Phase-Modulating Transmitter with Digital-to-Phase Converters and Constant-Envelope Phasors," IEEE RFIC, pp. 3-6, June 2025.
- [7] L. Piotto et al., "A 125-to-170GHz Power-Efficient Phase Shifter in SiGe BiCMOS with Outphasing Gain and Phase Corrections," ISSCC, pp. 546-548, Feb. 2025.
- [8] K. Kuliabin et al., "A 100–300 GHz Attenuator-Based Ultrawideband Vector Modulator," IEEE Trans. Terahertz Sci. Technol., vol. 14, no. 3, pp. 404-413, May 2024.
- [9] J. S.-C. Chien and J. F. Buckwalter, "A 110-120-GHz, 12.2% Efficiency, 16.2-dBm Output Power Multiplying Outphasing Transmitter in 22-nm FDSOI," IEEE ASSCC, pp. 1-3, Nov. 2022.
- [10] A. Standaert and P. Reynaert, "A 390-GHz Outphasing Transmitter in 28-nm CMOS," IEEE JSSC, vol. 55, no. 10, pp. 2703-2713, Oct. 2020.
- [11] T. LaRocca et al., "Millimeter-Wave CMOS Digital Controlled Artificial Dielectric Differential Mode Transmission Lines for Reconfigurable ICs," IEEE IMS, pp. 181-184, June 2008.
- [12] B. A. Abdelmagid et al., "A Wideband Bidirectional Calibration-Free Frequency/Switching-Staggering 360° D-Band Phase Shifter with Frequency-Invariant Codes Achieving <2.38°/0.63dB RMS-Errors Over 24% Bandwidth," ISSCC, pp. 548-550, Feb. 2025.
- [13] J. Zhou et al., "A 16-to-256QAM G-Band Subharmonic Phase-Modulating Transmitter for Beyond-5G Communications," ISSCC, pp. 354-356, Feb. 2026.

Nanoelectronic Artificial Intelligence Processors

CNF Project Number: 3169-24

Principal Investigator(s): Peter McMahon

User(s): Yongqi Zhang, Ruomin Zhu

Affiliation(s): Applied & Engineering Physics Department, Cornell University

Primary Source(s) of Research Funding: the David & Lucile Packard Foundation, Cornell AEP

Contact: pmcmahon@cornell.edu, cchen12@ucla.edu, yz2968@cornell.edu

Reserach Group Website: : <https://mcmahon.aep.cornell.edu/index.htm>

Primary CNF Tools: Westbond 7400A Ultrasonic Wire Bonder, KLA P7 Profilometer, YES EcoClean Asher, Oxford 81 RIE, Suss MA6|BA6 Aligner, Hamatech Hot Piranha, Oxford PECVD, Oxford 100 ICP Dielectric, Woollam RC2 Spectroscopic Ellipsometer, Zeiss Ultra SEMOxford 82 RIE 12

Abstract:

Analog computing using resistive crossbar arrays overcomes the von Neumann “memory wall” in digital computing, where data movement, instead of the computation itself, dominates the energy cost. By encoding weights in multi-level resistive cells and performing parallel dot-product operations directly within a 128×128 array fabricated at the Cornell Nanoscale Facility, we demonstrate up to 60.9 TOPS/W. This in-memory computing platform offers a compelling path toward dramatically lower-power AI inference, as well as efficient signal and image processing.

Summary of Research:

The explosive growth of AI services is driving data-center electricity demand toward unsustainable levels. The International Energy Agency projects global data-center energy use to exceed 945 TWh by 2030—more than double current levels—and U.S. data centers, already consuming 4.4 % of national electricity in 2023, may account for up to 12 % by 2028 [4][5]. Even a single Artificial Intelligence query carries a measurable footprint: a typical ChatGPT interaction consumes roughly 0.3 Wh, equivalent to running an LED bulb for several minutes [6].

Conventional von Neumann architectures exacerbate this burden via the “memory wall,” in which moving a 64-bit word from Dynamic Random Access Memory (DRAM) to the Central processing unit (CPU) costs on the order of 1,000 pJ—about $50\times$ the energy of a 64-bit floating-point add [7]. Across real workloads, data transfers can account for 60–70 % of total system energy, severely limiting both performance and efficiency.

Resistive crossbar arrays address this challenge by performing matrix-vector multiplications in situ: voltages applied to row lines induce column currents proportional to conductance-encoded weights, realizing

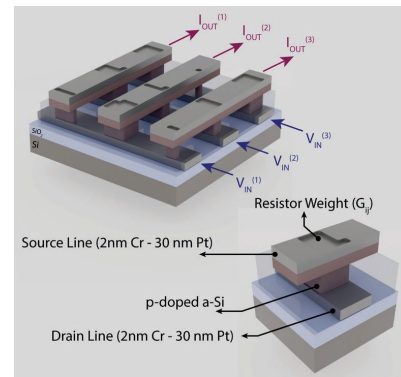


Figure 1: Structure of resistive crossbar arrays.

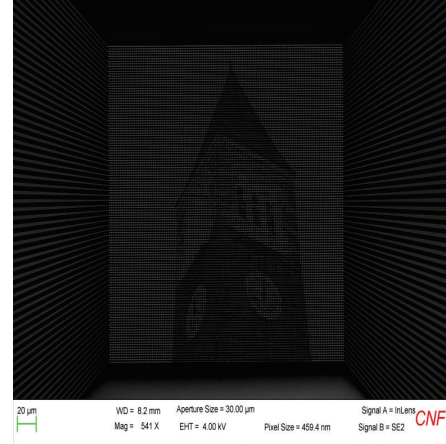


Figure 2: Fabrication picture.

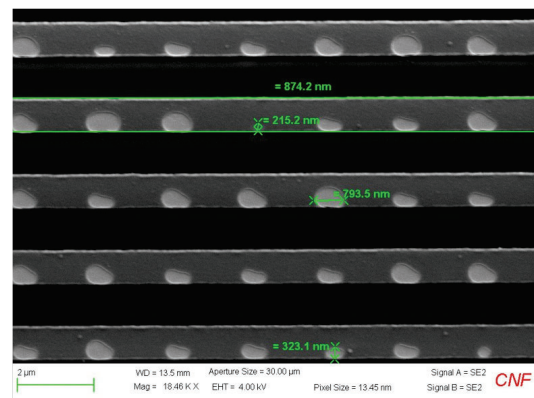


Figure 3: Device.

massively parallel dot products in one step. Hardware demonstrations include 60.9 TOPS/W for binary neural inference in oxide-based devices [1], 405 TOPS/W in magnetoresistive prototypes at 0.8 V [2], and 3.6 TOPS/W in designs with nonlinear Analog Digital Converters (ADCs) for specialized preprocessing [3].

In our work, we aim to fabricate resistive crossbar arrays with AI model encoded on them to save energy for AI computing. As a first step, we have fabricated 128×128 arrays using a CMOS-compatible process and measured their analog performance at Cornell Nanoscale Facility. By encoding a biosignal processing foundation model as conductance matrices and feeding input voltages corresponding to signals such as heart rate and movement, we obtained output currents that reproduce predictions on fall detection, sleep stage detection, stress level detection and atrial fibrillation (Fig. 4), validating hardware-in-the-loop processing as a viable digital alternative.

Digital & On-Chip Model Accuracy

Task	Input	Classification	Fully Digital	Partial hardware encoder + digital classifier
Atrial Fibrillation (AF) detection	Photoplethysmography (PPG), Electrocardiogram (ECG)	AF / not AF	85.9%	64.7%
Fall detection	Arm acceleration x, y, z	Falling / not falling	86.7%	80.1%
Sleep stage detection	Arm acceleration x, y, z	Wake / non rapid eye movement (REM) / REM	74%	44%
Stress level detection	ECG, Electrodermal activity (EDA), Respiration	Baseline / amused / stressed	69.7%	59.0%

Figure 4: Digital and Hardware processing results.

Conclusions and Future Steps:

We have shown that resistor-based crossbar arrays can achieve state-of-the-art energy efficiency for low-precision AI and image-processing tasks. To scale this approach, we plan to:

- Adjust array dimensions from a fixed 128×128 to customized based on the machine learning model we encode, enabling larger neural-network layers and more flexible model architecture.
- Expand application domains to voice-signal processing, discrete Fourier transforms and solving equations, leveraging the same in-memory dot-product primitive.

These developments will bring in-memory computing closer to deployment in edge AI accelerators and high-throughput signal-processing hardware.

References:

- [1] Li H, Wang S, Zhang X, Wang W, Yang R, Sun Z, Feng W, Lin P, Wang Z, Sun L, Yao Y. Memristive crossbar arrays for storage and computing applications. *Advanced Intelligent Systems*. 2021;3(9):n/a. doi:10.1002/aisy.202100017. Available from: <https://hdl.handle.net/2027.42/170211>
- [2] Jung S, Lee H, Myung S, Kim H, Yoon S-K, Kwon S-W, Ju Y, Kim M, Yi W, Han S, Kwon B, Seo B, Lee K, Koh G-H, Lee K, Song Y, Choi C, Ham D, Kim S-J. A crossbar array of magnetoresistive memory devices for in-memory computing. *Nature*. 2022;601:211–216. doi:10.1038/s41586-021-04196-6. Available from: https://ciqm.harvard.edu/uploads/2/3/3/4/23349210/jung2022.pdf?utm_source=chatgpt.com
- [3] Yang J, Mao R, Jiang M, Cheng Y, Sun P-S V, Dong S, Pedretti G, Sheng X, Ignowski J, Li H, et al. Efficient nonlinear function approximation in analog resistive crossbars for recurrent neural networks. *Nat Commun*. 2025;16:1136. doi:10.1038/s41467-025-56254-6. Available from: https://www.nature.com/articles/s41467-025-56254-6?utm_source=chatgpt.com
- [4] International Energy Agency. AI is set to drive surging electricity demand from data centres while offering the potential to transform how the energy sector works. IEA; 10 April 2025. Available from: https://www.iea.org/news/ai-is-set-to-drive-surging-electricity-demand-from-data-centres-while-offering-the-potential-to-transform-how-the-energy-sector-works?utm_source=chatgpt.com
- [5] Pomerleau S, Luna A. AI Data Centers: Why Are They So Energy Hungry? American Action Forum. July 15, 2025. Available from: https://www.americanactionforum.org/insight/ai-data-centers-why-are-they-so-energy-hungry/?utm_source=chatgpt.com
- [6] You J. How much energy does ChatGPT use? Gradient Updates, Epoch AI; 07 Feb 2025. Available from: https://epoch.ai/gradient-updates/how-much-energy-does-chatgpt-use?utm_source=chatgpt.com
- [7] Leland RL, Murphy R, Hendrickson B. Large-Scale Data Analytics and Its Relationship to Simulation. Executive Order of the President; January 2014. Available from: https://www.researchgate.net/figure/Energy-cost-in-picojoules-per-64-bit-floating-point-operation-for-various-common_fig4_312613278
- [8] Agarwal S, Quach T-T, Parekh O, Hsia AH, DeBenedictis EP, James CD, Marinella MJ, Aimone JB. Energy scaling advantages of resistive memory crossbar based computation and its application to sparse coding. *Frontiers in Neuroscience*. 2016;9:484. doi:10.3389/fnins.2015.00484. Available from: <https://www.frontiersin.org/journals/neuroscience/articles/10.3389/fnins.2015.00484/full>
- [9] Yin S, Sun X, Yu S, Seo J-S. High-Throughput In-Memory Computing for Binary Deep Neural Networks with Monolithically Integrated RRAM and 90 nm CMOS. *arXiv preprint arXiv:1909.07514*; 2019. doi:10.48550/arXiv.1909.07514. Available from: https://arxiv.org/abs/1909.07514?utm_source=chatgpt.com

Large-Area β -Ga₂O₃ Schottky Barrier Diodes with Sputtered NiO Edge Termination

CNF Project Number: 3238-25

Principal Investigator(s): Jonathan McCandless

User(s): Kazuki Nomoto

Affiliation(s): Gallox Semiconductors, Inc.

Primary Source(s) of Research Funding: Gallox Semiconductors, Inc.

Contact: jon@galloxsemi.com, kazuki@galloxsemi.com

Reserach Group Website: <https://www.galloxsemi.com/>

Primary CNF Tools: Heidelberg MLA 150 Maskless Aligner, Heidelberg Mask Writer DWL2000, Autostep i-line Stepper (GCA AS200), AJA sputter deposition tools, Oxford atomic layer deposition system, high-density-plasma chemical vapor deposition system, SC4500 electron-beam evaporators, P7 profilometer, Zeiss scanning electron microscope

Abstract:

Large-area vertical β -Ga₂O₃ Schottky barrier diodes (SBDs) incorporating sputtered nickel oxide (NiO) edge terminations were fabricated and evaluated. Four 1 mm-diameter anode layouts were compared: no edge termination, a continuous NiO termination, NiO with guard rings, and NiO with 20 guard rings plus an extended field plate. The devices were fabricated on (001) β -Ga₂O₃ samples thinned to <200 μ m. Capacitance-voltage measurements indicated a net donor concentration of approximately $1 \times 10^{16} \text{ cm}^{-3}$. All layouts showed similar forward conduction, while the NiO-based terminations substantially improved reverse blocking. The highest measured breakdown voltage approached 900 V, compared with less than approximately 300 V for unterminated diodes.

Summary of Research:

The objective of this work was to investigate an edge-termination process for large-area vertical β -Ga₂O₃ SBDs. Electric field crowding at the perimeter of a Schottky anode can cause premature breakdown and prevent the drift layer from supporting its expected voltage. Sputtered p-type NiO provides a deposited heterojunction termination that can redistribute the surface electric field without ion implantation into β -Ga₂O₃ [1-3].

Two 10 x 10 mm² samples were co-processed. The starting (001) β -Ga₂O₃ substrate was mechanically thinned to <200 μ m. The test mask contained sixteen 2 x 2 mm² dies and four device groups: SBDs without edge termination; SBDs with a continuous NiO edge

termination; SBDs with a continuous NiO region and NiO guard rings; and SBDs combining NiO, guard rings, and an extended metal field plate, as shown in figure 1. A metal oxide semiconductor capacitor was included as a dielectric control.

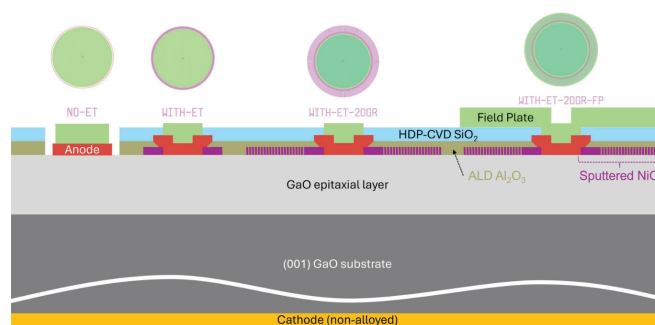


Figure 1: Cross-sectional schematics of the four vertical β -Ga₂O₃ SBD layouts: no edge termination, continuous NiO termination, NiO with 20 guard rings, and NiO with 20 guard rings plus an extended field plate.

The process began with liftoff patterning of sputtered NiO around the anode perimeter. An Al₂O₃ layer was then deposited by atomic layer deposition at 200°C and patterned to open the anode contact region. After anode metallization, SiO₂ was deposited by high density plasma chemical vapor deposition. The SiO₂ was opened above the anode, followed by field plate metallization and anode pad thickening. A non-alloyed cathode metal was deposited on the thinned backside. The completed sample showed good alignment of the large circular anodes, NiO rings, and field plate structures.

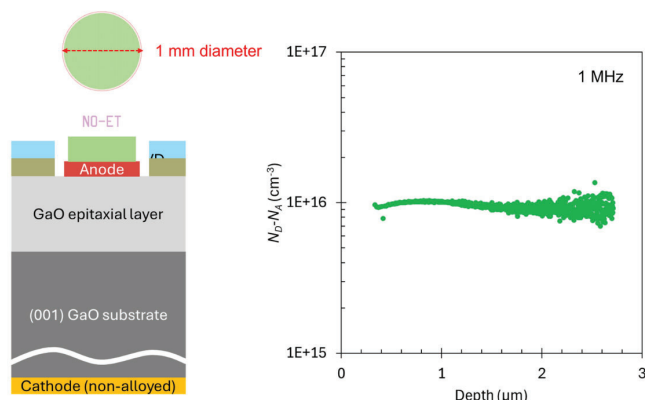


Figure 2: (a) CAD layout and photograph of the processed 10 x 10 mm² sample. (b) Net donor concentration extracted from 1 MHz capacitance-voltage measurements on a 1 mm-diameter diode.

In figure 2, capacitance-voltage measurements at 1 MHz on a 1 mm-diameter diode yielded a nearly uniform net donor concentration near 1×10^{16} cm⁻³ over the measured depletion depth. In figure 3, forward current-voltage characteristics were comparable among the four layouts, showing turn-on near 0.8 V and current density above 100 A/cm² at high forward bias. The minimum differential specific on-resistance was approximately 10–15 mΩ·cm², indicating that the added termination structures did not introduce a substantial forward conduction penalty.

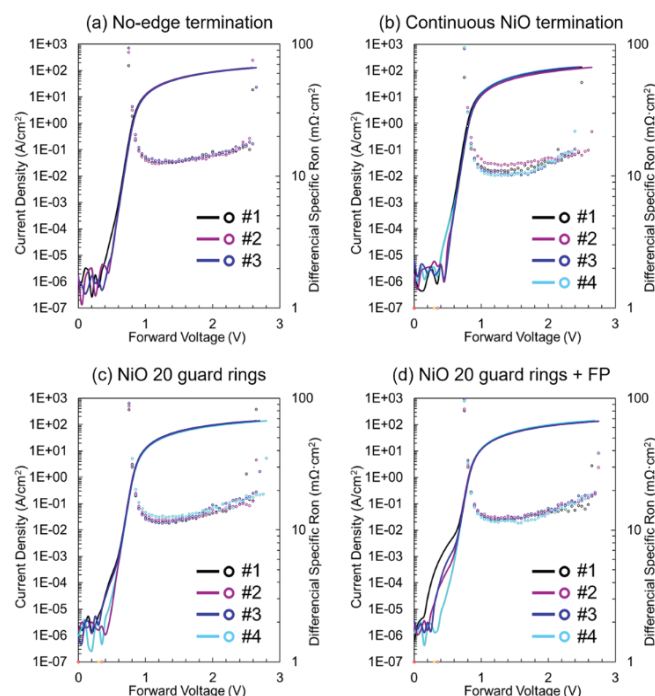


Figure 3: Forward current-voltage characteristics of the four termination designs. All designs exhibit comparable turn-on and high-current behavior, indicating a negligible forward-conduction penalty from the NiO termination structures.

Reverse characteristics were measured in insulating oil using a Keithley 2657A source measure unit, as shown in figure 4. Unterminated devices exhibited premature breakdown below approximately 300 V. Devices with a continuous NiO termination extended the blocking voltage into the 700 V range. Including guard-rings increased the breakdown to roughly 900 V.

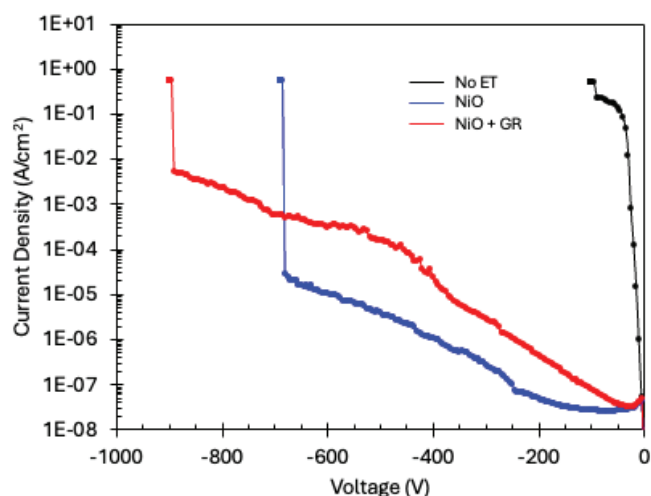


Figure 4: Reverse current-voltage characteristics and device locations. Measurements were performed in insulating oil using a Keithley 2657A. The best device approached breakdown of 900 V, whereas the unterminated control devices broke down below approximately 300 V.

Conclusions and Future Steps:

Sputtered NiO edge termination was successfully integrated with large-area vertical β -Ga₂O₃ SBDs and improved reverse blocking without degrading the forward characteristics. The results confirm that deposited NiO can reduce anode edge field crowding. Future work will optimize NiO conductivity and thickness, guard-ring spacing, dielectric quality, and field-plate overlap. A larger statistical data set, spatial correlation with pre-shipment wafer inspection maps, and post breakdown optical and electron-microscopy analysis will be used to distinguish design limitations from crystal- or process related failure sites.

References:

- [1] M. Xiao et al., "NiO junction termination extension for high-voltage (>3 kV) Ga₂O₃ devices", *Applied Physics Letters*, 122, 183501 (2023).
- [2] W. Hao et al., "Improved vertical β -Ga₂O₃ Schottky barrier diodes with conductivity-modulated p-NiO junction termination extension", *IEEE Transactions on Electron Devices*, 70, 2129-2134 (2023).
- [3] C. Liao et al., "Optimization of NiO/ β -Ga₂O₃ heterojunction diodes for high-power application", *IEEE Transactions on Electron Devices*, 69, 5722-5727 (2022).

Developing Novel Thermometry for Operating HEMTs

CNF Project Number: 3321-25

Principal Investigator(s): Zhiting Tian

User(s): Amelia Schaeffer, Lindsay Wright

Affiliation(s): Sibley School of Mechanical and Aerospace Engineering

Primary Source(s) of Research Funding: Defense Advanced Research Projects Agency

Contact: zt223@cornell.edu, afs97@cornell.edu, law289@cornell.edu

Reserach Group Website: <https://ztgroup.org/>

Primary CNF Tools: Everbeing EB-6 DC Probe Station, Veeco Icon AFM, Olympus MX-50 Microscope

Abstract:

As power densities of transistors continue to increase for high-frequency and high-power electronics, management of hotspots and heat withdrawal is becoming an increasingly important aspect of transistor and chip design. As such, the ability to measure device heating with high spatial and thermal resolution is highly desirable to advance device design, budgeting, and heat spreading systems. However, existing thermometry approaches are limited to being largely surface-sensitive or providing insufficient spatial resolution to measure sub-micron features within transistor structures. In this project we are developing a synchrotron-based X-ray diffraction imaging technique into a novel nanoscale thermometry method for operating high-electron-mobility transistors.

Summary of Research:

Prior to any attempted measurements of operating transistors by X-ray diffraction imaging, it is crucial to understand the structural and electronic properties of a transistor. As such, two major characterization approaches were taken at CNF to support our synchrotron-based measurements. The first is the characterization of specific device dimensions, chip layouts, metal contact thicknesses, and surface roughness in different device regions. These properties inform and enable X-ray diffraction-based imaging in different ways. Specific device dimensions and layouts were used to find a specific transistor to image within a larger chip even when in situ microscope imaging is not available, necessitating a blind alignment onto a device. Metal contact thickness, as measured by atomic force microscopy, allows a clearer understanding of the expected X-ray absorption contrast possible.

Surface roughness measurements were also extracted from atomic force microscopy for our ongoing efforts in integrating heat-spreaders into the device structure. An example of a transistor structure characterized for measurements by AFM is shown in Fig. 1.

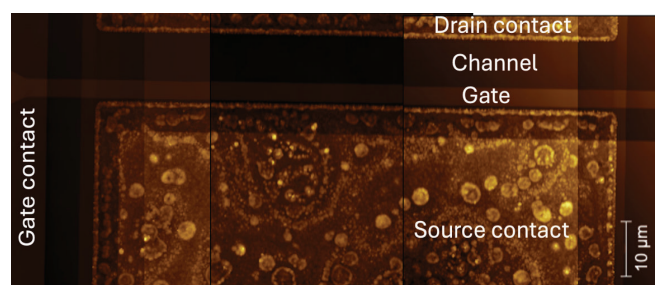


Figure 1: A high-resolution topographical map of a power transistor made from stitching together three atomic force microscopy images with regions of the device labeled. Quantifying the roughness of the annealed source and drain contacts is critical for designing effective heat spreader integration strategies.

The second class of characterization carried out for this project was electrical measurements of the transistors. Output and transfer curves were measured for transistors of different source-gate and gate-drain geometries to determine the relationship with current droop, which is caused by the device heating. Devices with higher current droop were selected for better visibility in X-ray thermal imaging, as well as to test the impact of placing heat spreaders on the devices. Preliminary measurements at CNF were compared with measurements during and after beam time at the Advanced Photon Source to monitor device health, as navigating measurement while avoiding X-ray induced damage is a major aim of the project. Fig. 2 shows output curve measurements made on the same device at different stages in the measurement process. It was found that this device remained operational after exposure to 20 keV X-rays but was damaged during heated measurements.

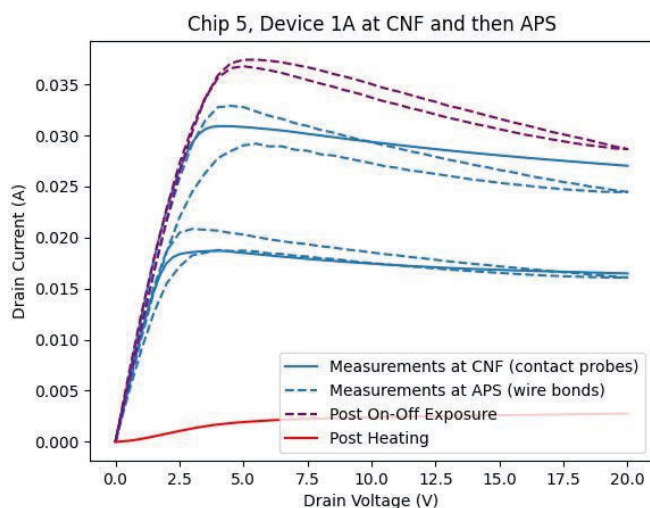


Figure 2: Output curves of a transistor device measured at beam time. Solid curves represent measurements completed at CNF and dotted curves represent measurements at the Advanced Photon Source during X-ray measurements. Monitoring these electrical measurements allows insight into changes throughout measurements.

Conclusions and Future Steps:

High-resolution spatial and topographical characterization has been completed through a combination of optical microscopy and atomic force microscopy to facilitate X-ray diffraction imaging of operating devices to develop temperature extraction methods. Electrical measurements of transistors exposed to various conditions has informed experimental design and data collection. Future work on this project involves analysis of data collected from synchrotron measurements, continuation of post-measurement characterization of the transistors to quantify any damage sustained, and development of heat spreaders that can be directly integrated into the device architecture.

Towards Quantitative Comparisons of Bulk and Local Optoelectronic Properties of Emerging Solar Cell Materials with Interdigital Electrodes

CNF Project Number: 86300

Principal Investigator(s): John A. Marohn

User(s): Azriel Finsterer

Affiliation(s): Cornell University Chemistry and Chemical Biology

Primary Source(s) of Research Funding: NSF Award DMR-2113994

Contact: john.marohn@cornell.edu, af482@cornell.edu

Primary CNF Tools: Hamatech Hot Piranha Cleaner, Hamatech developer tool, Class II Resist Spinners, Edge Bead Removal System, ABM Contact Aligner, Hamatech Wafer Processor, Oxford Plasma Etchers (81 and 82), SC4500 Odd-Hour Evaporator, SC4500 Even-Hour Evaporator, Disco Dicing Saw

Abstract:

Gold interdigitated electrodes were fabricated using a simple photolithography procedure. The electrodes were used in space charge-limited current (SCLC) experiments with a thin film of N,N'-Bis(3-methylphenyl)-N, N'-diphenylbenzidine embedded in a polystyrene matrix (TPD:PS). Optimized J–V curve acquisition parameters were determined and will be used in subsequent electric force microscopy (EFM) experiments to compare the bulk charge mobility of the TPD:PS from SCLC to the local charge mobility measured using EFM.

Summary of Research:

Organic photovoltaics (OPVs) and lead halide perovskites (LHPs) are two classes of photovoltaic materials that have attracted significant attention for their application in solar cell devices, with single-junction OPVs reaching 20% power conversion efficiency (PCE) as of 2025 and LHPs reaching 26.15% as of 2024, approaching the Shockley-Queisser limit [1–4]. Despite recent progress, there remain open questions about these materials, specifically the sub-Langevin charge recombination exhibited by OPVs and the generation of light-induced vacancies observed in LHPs [5–6]. Understanding these phenomena requires quantification of the local charge mobility. While novel electric force microscopy (EFM) measurements—a subclass of atomic force microscopy that detects electrostatic forces between a charged cantilever tip and sample—will be used to quantify local electronic properties, an established technique is needed to quantify the bulk charge mobility. Space charge limited current (SCLC) measurements can be used to determine the bulk mobility of a material and can be performed using fabricated gold interdigitated electrodes.

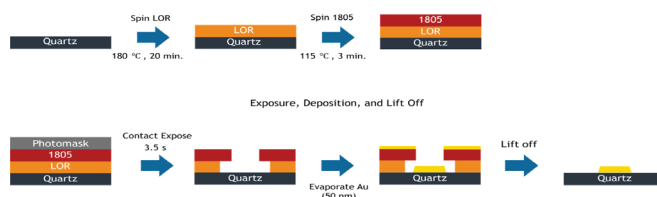


Figure 1: Schematic representation of the fabrication of gold interdigitated electrodes. Specific parameters are provided where possible.

Gold interdigitated electrodes were fabricated using a simple photolithography procedure shown in Figure 1 [7]. Four-inch quartz wafers (Mark Optics) were cleaned using hot piranha solution. The wafers were dehydrated at 180°C for 10 minutes and coated with LOR 1A resist (dynamic dispense at 400 rpm for 4 s, 4000 rpm for 45 s). The layer was soft-baked for 20 minutes at 180°C before S1805 resist was deposited statically (4000 rpm for 60 seconds, 1000rpm/s). The stack was soft-baked at 115°C for 3 minutes, and the edge bead was removed. The coated wafers were contact-exposed (ABM High-Resolution Contact Aligner) with near UV light for 3.5 s, with a corresponding dose range of 41.7 to 53.6 mJ/cm². The wafers were developed using AZ 762 Metal Ion Free developer with single-puddle spray development for 60 seconds (Hamatech). The resulting patterned wafer was descummed using an Oxford 81 Reactive Ion Etcher (50 mW, 30 s) before electrode deposition (5 Å Cr, 500 Å Au, 0.4 Å/s gold deposition rate). Lift-off was performed using 726 Metal Ion Free developer before dicing.

The fabricated electrodes were used in space charge-limited current (SCLC) experiments on the molecularly doped polymer system N,N'-Bis(3-methylphenyl)-N,N'-diphenylbenzidine in polystyrene (hereafter referred to as TPD:PS). This system is known to produce space charge-limited current and has a well-established bulk charge mobility [7–8]. TPD:PS thin films were spun onto

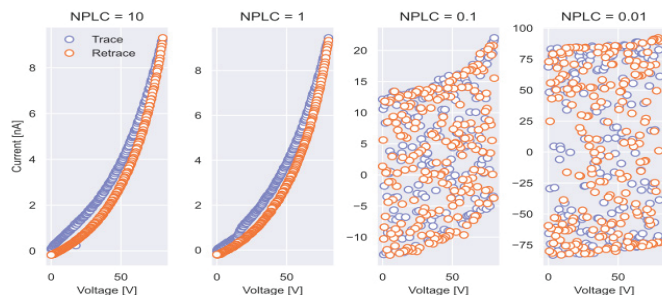


Figure 2: Current–Voltage curves for a *N,N'*-Bis(3-methylphenyl)-*N,N'*-diphenylbenzidine (TPD):polystyrene sample on gold interdigitated electrodes, varying the number of power line cycles (NPLC) used during data acquisition. The electrodes have a 12–micron separation and 1.5–mm length. All scans were taken with a constant voltage delay of 1 second.

interdigitated electrodes with a separation of twelve μm and a digit length of 1.5 mm using the protocol found in reference 7. Samples were loaded into a custom high–vacuum microscope where space charge–limited current measurements were performed using a Keithley 6430 source meter unit. Figures 2 and 3 show current–voltage curves collected as a function of voltage delay and number of power line cycles (NPLC). The optimum conditions were determined to be ten power line cycles and a voltage delay of 5 seconds. These conditions will be used for subsequent EFM experiments in the space charge limit.

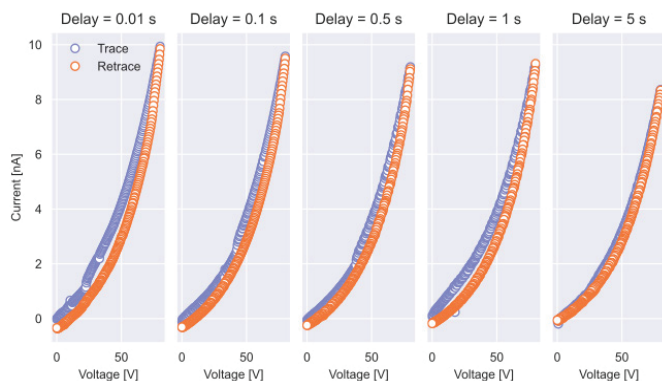


Figure 3: Current–Voltage curves for a *N,N'*-Bis(3-methylphenyl)-*N,N'*-diphenylbenzidine (TPD):polystyrene sample on gold interdigitated electrodes, varying the voltage delay used during data acquisition. The electrodes have a 12–micron separation and 1.5–mm length. All scans were taken with a constant NPLC of 10.

Conclusions and Future Steps:

Gold interdigitated electrodes were fabricated using a simple photolithography procedure. Space charge–limited current experiments on the molecularly doped polymer TPD:PS were performed, and space charge–limited current was directly observed as a non–linearity in the current–voltage curve. Changing the scan speed of the experiment by varying the NPLC and voltage delay revealed the optimal conditions of ten PLC and a five–second voltage delay. These conditions will be used in future experiments to determine the bulk charge mobility of the conductive polymer system, which will be compared to the local charge mobility quantified from novel EFM measurements.

References:

- [1] Shockley, W. and Queisser, H.J. J. Appl. Phys. 32, 510–519 (1961) .
- [2] K. Walzer, B. Maennig, M. Pfeiffer, and K. Leo, “Highly Efficient Organic Devices Based on Electrically Doped Transport Layers,” Chem. Rev. 107(4), 1233–1271 (2007).
- [3] H. Chen, C. Liu, J. Xu, A. Maxwell, W. Zhou, Y. Yang, Q. Zhou, A. S. R. Bati, H. Wan, Z. Wang, L. Zeng, J. Wang, P. Serles, Y. Liu, S. Teale, Y. Liu, M. I. Saidaminov, M. Li, N. Rolston, S. Hoogland, T. Filleter, M. G. Kanatzidis, B. Chen, Z. Ning, and E. H. Sargent, Improved charge extraction in inverted perovskite solar cells with dual–site–binding ligands, Science, 2024, 384, 189–193, URL <https://doi.org/10.1126/science.adm9474>.
- [4] L. Wang, C. Chen, Z. Gan, J. Cheng, Y. Sun, J. Zhou, W. Xia, D. Liu, W. Li, and T. Wang, Diluted Ternary Heterojunctions to Suppress Charge Recombination for Organic Solar Cells with 21% Efficiency, Adv. Mater., 2025, 37, 2419923, URL <https://doi.org/10.1002/adma.202419923>.
- [5] Langevin, P. Ann. Chim. Phys. 28, 433 (1903).
- [6] Tirmzi, A.M., Dwyer, R.P., Hanrath, T. and Marohn, J.A. ACS Energy Lett. 2017, 2, 488–496.
- [7] Silveira, W. R.; Marohn, J. A. Microscopic View of Charge Injection in an Organic Semiconductor. Phys. Rev. Lett. 2004, 93 (11), 116104. <https://doi.org/10.1103/PhysRevLett.93.116104>.
- [8] Murgatroyd, P. N. Theory of Space–Charge–Limited Current Enhanced by Frenkel Effect. J. Phys. D: Appl. Phys. 1970, 3 (2), 151. <https://doi.org/10.1088/0022-3727/3/2/308>.

Metal-Oxide Interface Preservation Using Atomic Layer Deposited Metal Interlayers

CNF Summer Student: Lincoln Hogan

Student Affiliation: Department of Electrical and Computer Engineering, North Carolina State University

Summer Program(s): 2026 Cornell NanoScale Facility Research Experience for Undergraduates (CNF REU) Program

Principal Investigator(s): Grace Xing, Cornell University

Mentor(s): Joseph Dill

Primary Source(s) of Research Funding: SUPREME, National Science Foundation under Grant No. NNCI-2025233

Contact: ldhogan@ncsu.edu, grace.xing@cornell.edu, jed296@cornell.edu

Summer Program Website(s): <https://www.cnf.cornell.edu/education/reu/2026>

Abstract:

Energetic metal deposition techniques have been shown to introduce defects at the metal-oxide (MO) interface, degrading the electrical performance of gate dielectrics in MOS structures. In this work, we compare MO interface degradation resulting from conventional energetic metallization techniques with that of atomic layer deposited (ALD) gate metals. We demonstrate that fully in-situ ALD dielectric and metal deposition provides minimal improvement over post-passivation ALD metallization, indicating that air exposure following ALD passivation does not significantly degrade interface quality. Finally, we show that thin ALD gate metals preserve the MO interface during subsequent energetic metal deposition, enabling additional metallization without measurable degradation of dielectric performance. These results demonstrate that thin ALD metal interlayers provide an effective strategy for preserving MO interface quality while maintaining flexibility in subsequent metallization processes and material selection.

Summary of Research:

Energetic Physical Vapor Deposition (PVD) gate metallizations have been shown to degrade dielectric quality through the introduction of defect states [1]. X-Ray and UV radiation from Magnetron Sputtering and Electron-Beam Evaporation (EBE) can break dielectric bonds. Argon ions from Sputter plasma embed themselves deep in the dielectric [1]. According to the Multiphonon Trap Assisted Tunnelling (TAT) theory, Fowler-Nordheim (FN) TAT is maximized when defect states lie 29.3% of the tunnelling barrier distance away from the cathode (x^*) [2], [3]. Interface trap states can also increase TAT by lowering the effective barrier at the Metal-Oxide (MO) interface (Φ_{MO}) as seen in Fig. 1. Higher initial tunnelling current (I_0) results in earlier

time-to-breakdown (tBD) due to a higher population of lucky electrons as shown in Fig. 2 [2]. This means that the more penetrative the deposition is, the faster the device will break.

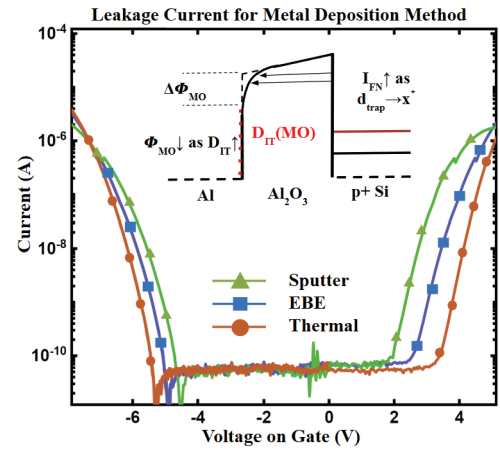


Figure 1: I-V sweeps on 180 μm DIA pads on 15 nm Al_2O_3 . Traps at the MO interface lower the effective barrier Φ_{MO} . Sputtering results in the earliest onset current due to high DIT (- bias) and deep drap (+ bias).

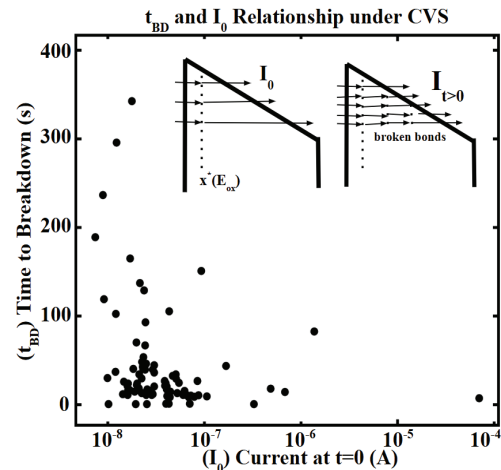


Figure 2: Time-to-breakdown is plotted against initial leakage current at constant voltage stress (CVS). It is shown that higher tBD is achieved when I_0 is low. High defect density at x^* results in maximized I_0 .

We fabricate nine Al/Al₂O₃/p+Si MOS capacitors with varied metallization methods. C-V measurements show oxide capacitance (C_{ox}) remains comparable between the samples, indicating Al₂O₃ thickness and dielectric constant (ϵ_{ox}) are unchanged. In Fig. 1 our I-V plot confirms literature reports that Sputtering results in the earliest onset TAT, followed by EBE and Thermal Evaporation [1]. Positive bias likely represents increased FN current due to barrier lowering, while negative bias likely indicates trap-limited Frenkel-Poole (FP) tunnelling. Three Thermally Evaporated samples are produced with 30, 15, and 5 nm oxides to access thickness dependence. C-V measurements confirm a plausible Density of Interface Traps (DIT) and C_{ox} thickness trend, J-E leakage plots showed no dependence on thickness, further indicating that leakage through the Al₂O₃ is largely governed by interfacial defects.

After the energetic PVD study we fabricate TiNx/Al₂O₃/p+Si MOS capacitors with ALD metallization. J-E plots showed almost 2x increase in negative bias TAT onset field for ALD metallization compared to Thermal. The 0.5 eV increase in Φ_{MO} from Al to TiNx is not relevant to our J-E negative sweeps which are largely dominated by trap-limited FP tunnelling. FN tunnelling still occurs, but the tunnelling barrier is too thick for Φ_{MO} to be rate-limiting. Time-dependent dielectric breakdown (TDDB) measurements under constant voltage stress (CVS) in Fig. 3 confirm that ALD metallization yields higher tBD when compared to Thermal. This likely arises from the significantly lower leakage current I₀ in the ALD sample [2].

Despite its proven advantages, the cost, processing time, and material limitations of ALD have hindered its widespread adoption as a gate metallization technique. We demonstrate that integrating a thin ALD metallization layer between dielectric deposition and conventional PVD metallization enables broader process compatibility while preserving MO interface integrity. We compare EBE Cr (150nm) deposited on TiNx (40 nm) and Al₂O₃ (7 nm) ALD films grown under vacuum with an identical film that was exposed to atmosphere between Al₂O₃ and TiNx. We additionally compare a vacuum-deposited TiNx/Al₂O₃ film with no EBE Cr. Weibull analysis in Fig. 4 reveals no variation in tBD or Weibull slope (β) between the three samples. Additionally, negative field J-E sweeps appear consistent across samples. From this analysis we can infer that the MO interface is protected from EBE by 40 nm TiNx and oxygen defects at the MO surface have little impact on tunnelling current. This follows our earlier framework, as oxygen defects are significantly shallower than x* [3].

In this work we demonstrate dielectric quality degradation across various energetic PVD methods [1] and compare an example of ALD metallization. We have shown that 40 nm TiNx can be deposited on Al₂O₃ after air-transfer and prior to EBE of Cr while still preserving the metal-oxide interface. This work establishes the foundation for ALD interlayer engineering. Future studies should determine the minimum effective interlayer thickness and evaluate compatibility with a broader range of metallization schemes, ultimately enabling a universal metal-oxide interface protection layer.

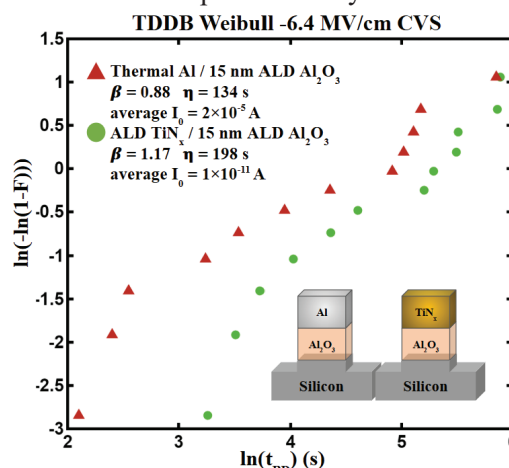


Figure 3: TDDB under CVS at -6.4MV/cm (~90% of EBD). Weibull slope (β) was poor but comparable between samples. The intrinsic time-to-breakdown lifetime (η) increased 47% from Thermal to ALD, while early breakdown times increased almost 177%. We observe 6 orders of magnitude decrease in current at $t = 0$ from Thermal to ALD.

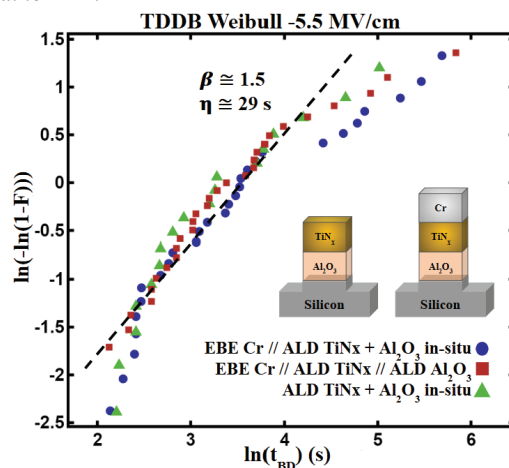


Figure 4: TDDB measurements are performed under constant voltage stress (CVS) at -5.5MV/cm (~90% of EBD). Weibull slope (β) and intrinsic time-to-breakdown lifetime (η) remain consistent across each sample. No change in leakage I₀ was observed.

References:

- [1] I. Mack et al., "Quantifying the Impact of Al Deposition Method on Underlying Al₂O₃/Si Interface Quality," Phys. Status Solidi.
- [2] Z. Chbili et al., "Modeling Early Breakdown Failures of Gate Oxide in SiC Power MOSFETs," IEEE Trans. Electron Devices.
- [3] S. Makram-Ebeid and M. Lannoo, "Quantum Model for Phonon-Assisted Tunnel Ionization of Deep Levels in a Semiconductor," Phys. Rev.

Thermomechanical Nanomolding of Single Crystalline CoSn Nanowires

CNF Summer Student: Bruce Pan

Student Affiliation: College of Chemistry, University of California, Berkeley

Summer Program(s): 2026 Cornell NanoScale Facility Research Experience for Undergraduates (CNF REU) Program

Principal Investigator(s): Judy J. Cha, Cornell University

Mentor(s): Jack Coyle

Primary Source(s) of Research Funding: SUPREME, National Science Foundation under Grant No. NNCI-2025233

Contact: judy.cha@cornell.edu, bdp@berkeley.edu, jdc384@cornell.edu

Summer Program Website(s): <https://www.cnf.cornell.edu/education/reu/2026>

Research Group Website: cha.mse.cornell.edu

Primary CNF Tools Used: Nabity NPGS Nanometer Pattern Generator System; Carl Zeiss GeminiSEM 560 scanning electron microscope

Abstract:

Copper interconnect resistivity climbs as line dimensions shrink because electrons scatter at surfaces and grain boundaries. CoSn is a kagome metal that carries current more easily along the *c* direction than in the basal plane, which makes *c* direction CoSn nanowires worth evaluating as a replacement conductor. This project used thermomechanical nanomolding to press bulk CoSn into nanoporous anodic aluminum oxide and release wires in dilute hydrofluoric acid. Scanning transmission electron microscopy found many single crystal wires with [001] long axes, and energy dispersive X ray spectroscopy returned normalized fractions of 50.64 atomic percent cobalt and 49.36 atomic percent tin. Four terminal devices were built on single wires, but rectifying contacts prevented extraction of an intrinsic resistivity.

Summary of Research:

Cobalt atoms in CoSn sit on kagome nets stacked along the *c* axis, which produces flat bands near the Fermi level [4]. Single crystal measurements put the basal plane resistivity more than an order of magnitude above the *c* axis value [5], and films reach about 13 microhm centimeters along *c* [6]. Neither geometry shows how resistivity behaves once the conductor is confined to a nanoscale cross section [7]. The aim was to mold *c* direction single crystal nanowires and measure them individually.

Feedstock was pressed against a nanoporous anodic aluminum oxide template at 550 degrees Celsius and 250 megapascals for two hours, so metal fills the pores by pressure driven diffusion rather than melting [1,2,3]. The template was dissolved in 5 weight percent hydrofluoric acid and the wires sonicated and drop cast onto marked substrates. Of five molding runs, CS4 yielded nothing, which we attribute to insufficient effective pressure.

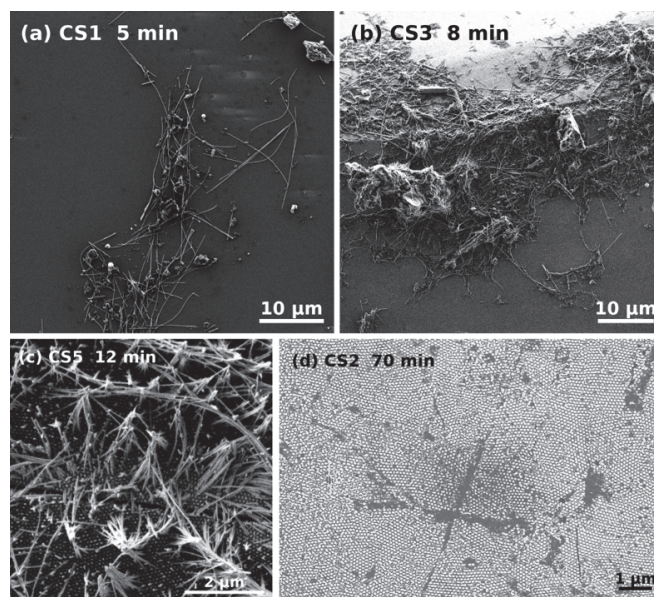


Figure 1: Released material after 5, 8, 12 and 70 minutes in 5 weight percent hydrofluoric acid. Twelve minutes gave the cleanest dense arrays in this sample set.

Release time controls how much product survives, and Figure 1 brackets it. Five minutes left sparse fragments in undissolved template. Eight minutes freed more material but left it matted in residue. Twelve minutes gave the cleanest dense arrays. Seventy minutes removed the wires and left only stubs. Filling fraction, delamination and handling also varied between runs, so this is a usable window rather than a universal optimum.

Scanning electron microscopy showed structures several micrometers long at the 40 nanometer nominal diameter set by the template. One frame gave an apparent width of 52.19 nanometers, which we did not treat as physical because aperture and stigmatism were not optimized. Collaborator imaging at the Cornell Center for Materials Research resolved the lattice directly. Figure 2 shows wires along [120] and [110], both single crystalline with [001] long axes, so many wires grow with the fast axis

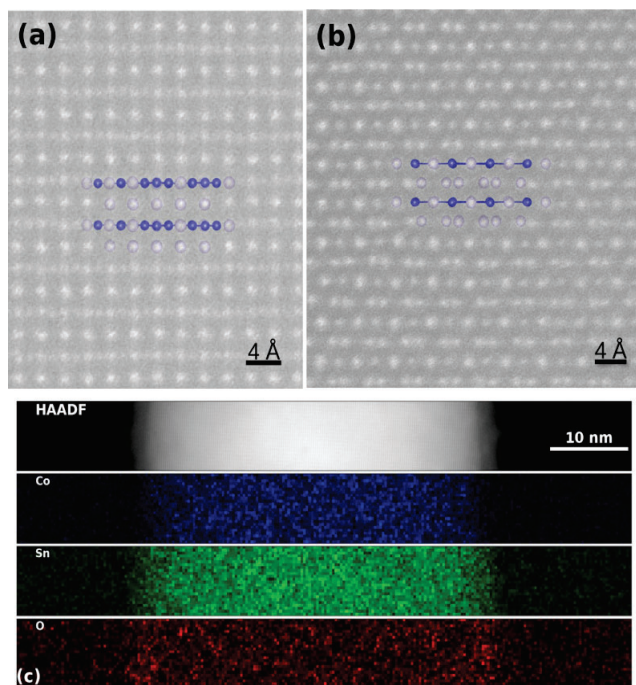


Figure 2: Atomic resolution high angle annular dark field imaging of single crystal CoSn nanowires along $[120]$ in (a) and $[110]$ in (b), both with $[001]$ long axes, with elemental maps across a wire cross section in (c) showing cobalt and tin in the core and oxygen at the surface.

along the wire. Elemental maps confirm cobalt and tin throughout the core. Quantification normalized to those two elements gave 50.64 and 49.36 atomic percent, each with 3.17 percent reported error, consistent with 1:1 stoichiometry. Oxygen at the surface suggests a thin tin oxide shell of undetermined thickness.

Four electrodes were patterned across a single wire by electron beam lithography on the Nabity Nanometer Pattern Generator System at the Cornell NanoScale Facility, with contact metal deposited at the Cornell Center for Materials Research. Inner probe spacing was 2.49 micrometers. Figure 3 shows a completed device and the most common failure mode, where the wire dislodges during processing and the electrodes land on bare substrate. Yield was limited more by wire retention than by lithography.

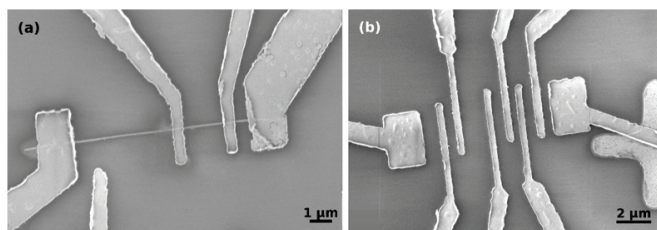


Figure 3: Four terminal device on a single CoSn nanowire in (a), and in (b) a set of electrodes left with no wire after the wire was dislodged during processing.

Electrical testing used a Keysight B1500A parameter analyzer. Two point sweeps between contact pairs are collected in Figure 4. Most pairs were close to linear over plus or minus 100 nanoamperes, which initially suggested usable contacts, but one pair rectified strongly and is plotted against the right hand axis. Alternating current measurement then identified one contact as Schottky and returned roughly 12 megohms of apparent four terminal impedance. Because drive frequency, amplitude and phase were not retained, that number cannot be assigned as a resistance. Other devices were also nonohmic, so no intrinsic resistivity or contact resistance was extracted.

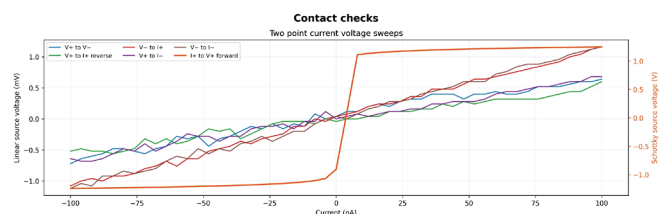


Figure 4: Two point current voltage sweeps between contact pairs. The rectifying pair uses the right hand axis. Alternating current measurement later identified one Schottky contact on this device.

Conclusions and Future Steps:

Nanomolding produced long CoSn nanowires, microscopy confirmed many single crystal wires with $[001]$ long axes and the expected composition, and four terminal device fabrication was demonstrated. The contacts, not the supply of wires, stopped the transport measurement. Next steps are to treat the wire surface before metal deposition, improve wire adhesion during processing, check every contact pair for ohmic behavior before a four terminal sweep, and keep the full alternating current settings and raw data. Resistivity can then be measured across several diameters to test scaling directly.

References:

- [1] Z. Liu et al., "Nanomolding of Crystalline Metals: The Smaller the Easier," *Physical Review Letters* 122, 036101 (2019).
- [2] N. Liu et al., "General Nanomolding of Ordered Phases," *Physical Review Letters* 124, 036102 (2020).
- [3] M. T. Kiani and J. J. Cha, "Nanomolding of Topological Nanowires," *APL Materials* 10, 080904 (2022).
- [4] M. Kang et al., "Topological Flat Bands in Frustrated Kagome Lattice CoSn," *Nature Communications* 11, 4004 (2020).
- [5] H. Huang et al., "Flat-Band-Induced Anomalous Anisotropic Charge Transport and Orbital Magnetism in Kagome Metal CoSn," *Physical Review Letters* 128, 096601 (2022).
- [6] T. Nakatani et al., "Fabrication and Characterization of Single-Crystalline CoSn (10–10) Kagome Metal Thin Films for Interconnect Applications: Structure and Anisotropic Electrical Resistivity," *Applied Physics Letters* 127, 203302 (2025).
- [7] M. T. Kiani and J. J. Cha, "Shrinking Interconnects beyond Copper," *Science* 390, 572 to 573 (2025).