

Investigating the Impact of an External Electric Field on Thermal Behavior

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Primary CNF Tools Used: ABM Contact Aligner, SUSS MA6-BA6 Contact Aligner, SC4500 Odd-Hour Evaporator, Glen 1000 Resist Strip, Everbeing EB-6 DC Probe Station

Abstract:

As electronics continue to scale to smaller dimensions and increased power densities, understanding how electric fields impact the thermal properties of materials becomes important for accurate thermal budgeting. In this work, we fabricate structures to study how thermal properties of hexagonal boron nitride (h-BN) change when a cross-plane electric field is applied to the material. Microscale metal-insulator-metal structures with Ti/Au contacts were fabricated using dry transfer, contact photolithography, electron-beam evaporation, and liftoff processing. Measurement and analysis of the thermal conductivity and thermal boundary conductance of the h-BN flakes during DC electrical biasing is ongoing.

Summary of Research:

To perform thermal measurements, a lateral h-BN flake dimension of at least 80 μm is desirable, and thicker flakes are selected to help limit the influence of the interfaces on thermal measurements. Bulk samples are not used since a single-crystal domain is necessary to eliminate the effect of grain boundaries. Additionally, the voltage sources required to apply significant electric fields across bulk crystals are significantly more hazardous than those that can be used to apply high fields when a thin crystalline flake is used. Compared to typical 2D material flakes used for device fabrication, these flakes have much larger lateral dimensions ($\sim 100\ \mu\text{m}$ x $\sim 100\ \mu\text{m}$) and are thicker (100 nm to 100 nm). This,

combined with the electrode dimensions, allows us to utilize contact photolithography to pattern our electrodes, a technique not typically used for 2D flakes.

Mask design, mask writing, and photolithography dose testing were all performed as initial steps in the device development process. To make a wafer of devices, the bottom electrodes are patterned, metal is deposited, and liftoff is performed. A bottom electrode thickness of 40 nm (10 nm Ti adhesion layer, 30 nm Au) was used to minimize the step edge the flake needed to be draped over while still giving a mechanically robust bottom electrode for further processing and testing. The minimization of the step edge helps to prevent air bubble formation and flake delamination during device fabrication. After the bottom electrode is set, standard dry transfer techniques are used to precisely place h-BN flakes onto the bottom electrode. Then, the top electrode is patterned on top of the flake, and deposition and liftoff are repeated. Sonication cannot be used at any step once the flakes are placed, as it can lead to delamination. An example of a fully fabricated device is shown in Figure 1.

Iteration on this general process was necessary to ensure repeatable and high-quality results. The initial wafer of devices run showed contaminants on the flake that affected the top electrode, and atypical aging of the gold used for both the top and bottom electrodes was observed. An oxygen plasma resist strip and a more aggressive substrate clean prior to processing resolved these two issues, respectively.

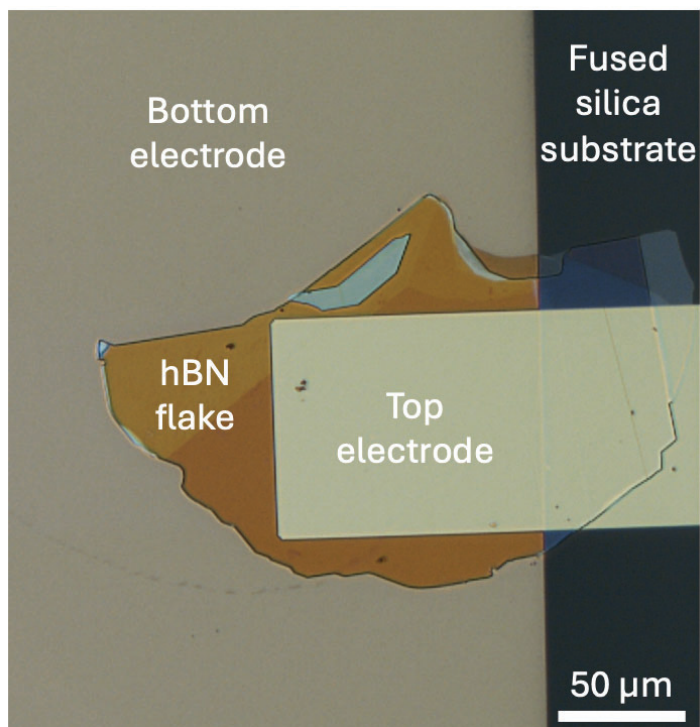
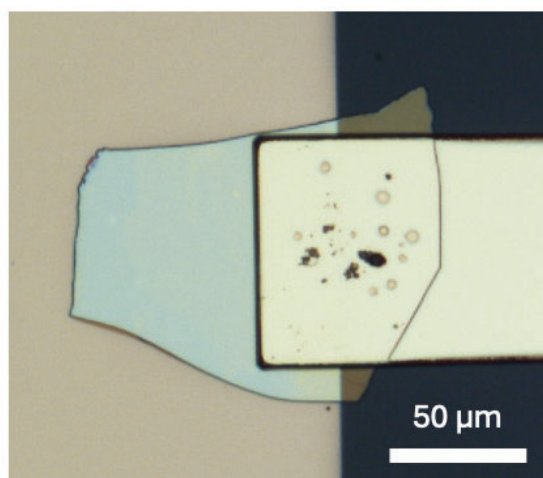


Figure 1: An optical microscope image of a fully-fabricated device with structures labelled for clarity. Both the top and bottom electrodes are Au with a Ti adhesion layer, but the difference in electrode color in the microscope image is due to the different thicknesses of Au used in the top and bottom electrodes.

Conclusions and Future Steps:

A repeatable and effective fabrication method has been developed for these devices that ensures well-defined contacts and clean surfaces. These devices are now undergoing thermal measurements while fields are applied, and future steps will be informed by the experimental results obtained from these measurements.

First Wafer



Second Wafer

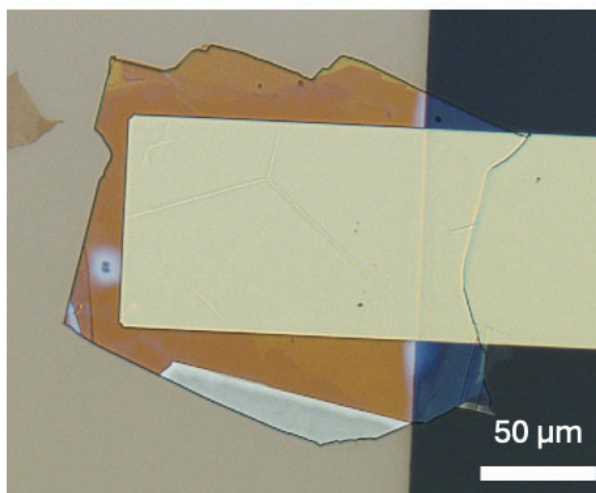


Figure 2: Two optical microscope images showing a device on the first wafer fabricated without additional cleaning steps and a device on the second wafer where more robust substrate cleaning and an oxygen plasma clean immediately prior to top electrode deposition helped to eliminate residues present on the first wafer.