

SUPREME Tasks 6/7

CNF Project Number: 3078-23

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Primary CNF Tools Used: SUSS MA6-BA6 Contact Aligner, Unaxis 770 Deep Silicon Etcher, AJA Ion Mill, AJA Sputter Deposition, Veeco Savannah ALD, Electroplating Hood – Au/Cu, P7 Profilometer, Zygo Optical Profilometer, Pico MA FinePlacer FlipChip Bonder, HFTL DC Probe Station, HFTL Small-Signal Probe Station, HFTL Terahertz Small-Signal Probe Station, PlasmaTherm Singulator, Logitech Orbis CMP

Abstract:

As the demand for heterogeneous integration for RF chiplets continues to grow, through-substrate vias (TSVs) with low loss at millimeter-wave frequencies have become increasingly important. In this study, we investigate TSVs through 200- μm -thick Si interposers. The Si wafers are first thinned and patterned, followed by TSV formation using the Bosch deep reactive ion etching (DRIE) process. The TSV sidewalls are subsequently metallized with Pt by atomic layer deposition (ALD) and filled with electroplated Cu. To enable heterogeneous integration, fine-pitch Cu pillars are fabricated and electrically characterized. Cu pillars approximately 50 μm in diameter and 13- μm high, exhibit a DC series resistance below 1 Ω . Separately, to demonstrate millimeter-wave heterogeneous integration, a GaN-on-Si chiplet with Cu pillars is thermocompression-bonded onto a SiC interposer with Au contacts. The resulting Cu-Au interconnects exhibit a series resistance below 1 Ω , confirming the viability of the proposed interconnect technology for heterogeneous integration of millimeter-wave circuits.

Summary of Research:

To demonstrate Si interposer fabrication and to establish a robust process flow, we use thinned 150-mm high-resistivity (HR) Si wafers with a thickness of approximately 200 μm and a resistivity greater than 5 $\text{k}\Omega\cdot\text{cm}$. Each Si wafer is initially thinned using the PT Singulator. Once the DISCO grinder becomes available, this thinning step will be transitioned to the DISCO system to achieve smoother surface. 50-nm-thick Al_2O_3 is subsequently deposited on the backside of the wafer using the AJA sputter deposition system. Al_2O_3 was selected as hard mask because of its 1000:1 selectivity during the Bosch DRIE process of alternating C_4F_8 and SF_6 gases. Currently, TSVs are fabricated using the UNAXIS 770 Deep Silicon Etcher. As the fabrication

process matures, this step will be transition to the PlasmaTherm Singulator platform.

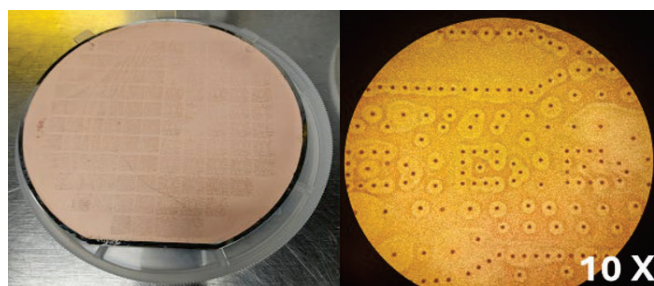


Figure 1: (a) Micrograph of Cu-plated 150-mm HR Si wafer and (b) detailed view of TSVs.

After the TSVs are completely etched, ALD is used to conformally deposit a Pt seed layer on the TSV sidewalls. Cu is then electroplated to fill the TSVs (Fig. 1). Following the backside processing, the front side of the wafer is patterned into Ti/Al transmission lines using the AJA sputter deposition system. The fabrication sequence and completed Si interposer structure are shown in Fig. 2.

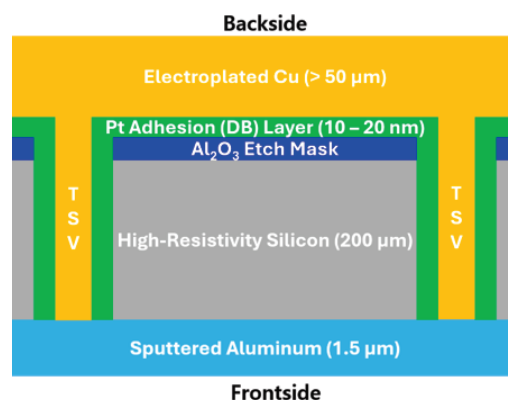


Figure 2: Si interposer cross-section schematic.

Cu pillars are fabricated on a Si substrate using a 200-nm Pt seed layer. A photoresist mold was formed using SPR220 photoresist and an image-reversal process to create an undercut profile. Copper is then electroplated to form cylindrical pillars with diameters of approximately 50 μm and heights of approximately 13 μm (Fig. 3). Electrical characterization shows that the fabricated Cu-pillar interconnects have a series resistance below 1 Ω , demonstrating their suitability for low-resistance, fine-pitch flip-chip integration.

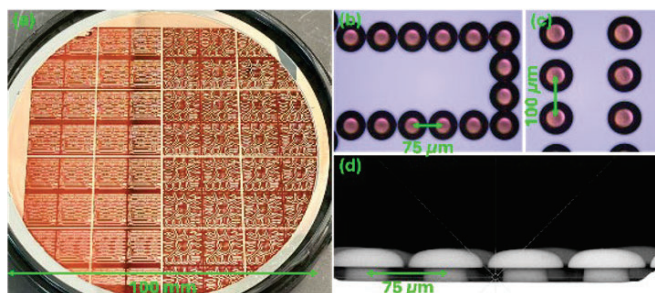


Figure 3: (a) Optical top view of a 100-mm Si wafer electroplated with Cu. (b) Optical top view and SEM side view of Cu pillars.

For RF heterogeneous integration, a GaN-on-Si chiplet is flip-chip bonded onto a SiC interposer through Cu-Au contacts using thermocompression bonding at 350 $^{\circ}\text{C}$ with an applied bonding force of 5 N for 5 min (Fig. 4). The resulting Cu-Au interconnects exhibited a series DC resistance below 1 Ω .

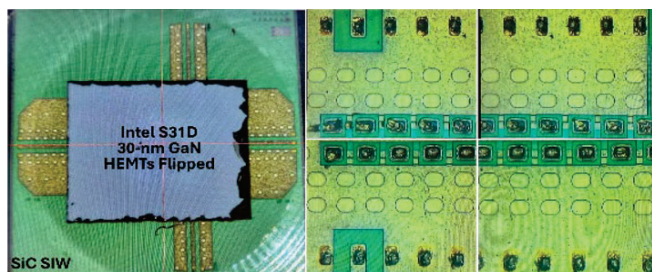


Figure 4: Top-view micrographs of (a) a GaN-on-Si chiplet flip-chip-bonded on a SiC interposer and (b) uniform footprints on the interposer after removal of the chiplet.

Conclusions and Future Steps:

The fabrication of Si interposers focused on optimizing the Bosch DRIE process for thin HR Si wafers and refining the metallization process to achieve uniform anisotropic TSV etching and reliable Cu filling across the wafer. With upgraded fabrication capabilities and an improved design incorporating on-wafer calibration standards, TSV-grounded transmission lines are expected to achieve a new state of the art performance with insertion loss below 0.5 dB/mm up to 140 GHz. Their RF performance will be characterized using HFTL's 220-GHz single-sweep probe station.

The demonstrated low-resistance Cu-pillar interconnects and successful GaN-on-Si flip-chip bonding onto SiC interposers confirm the feasibility of heterogeneous integration for millimeter-wave transceiver frontends. Future work will focus on fabricating finer-pitch Cu pillars on SiC, HR Si, and AlN interposers, followed by comprehensive small-signal millimeter-wave characterization of the flip-chip interconnects and heterogeneously integrated GaN-on-Si chiplet on SiC interposer.