

# Bonding 4in Silicon Wafers

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*Primary CNF Tools Used: MOS Clean Bench & Tanks, Schott IR Inspector, Suss SB8e Substrate Bonder*

## Abstract:

Geegah is investigating ultrasonic imaging of embedded patterns at the bonded interfaces. Bonded Silicon wafers are a useful tool for exploring embedded patterns in Silicon. Here we present our initial development efforts to evaluate the bond quality between unpatterned wafers.

## Summary of Research:

Two double side polished wafers were used for the bonding process. It was critical that the wafers had a bow of less than 30 micrometers and total thickness variation (TTV) of less than 5 micrometers [1][2][3]. The commercial wafers that were used during these experiments had a bow of less than 10 micrometers.

The two Silicon wafers were prepared by first processing in the MOS clean station followed by the spin rinse dryers. Bond quality is highly dependent on surface cleanliness. The wafers were cleaned in a fresh MOS clean station chemical batch to ensure a high-quality clean.

After the MOS cleaning, the wafers were immediately placed into the SB8e bonder. The 0anodic\_BPSG\_Si\_NOSPACERS recipe was used. This heated the chamber to 100 °C, vacuumed down to five millibar, heated up to 300 °C, and then forced the wafers together. The step where voltage was applied to the wafers was skipped since it shorted the high voltage supply and caused the recipe to time out. The bonded wafers can be removed from the chamber after the cooling process has completed.

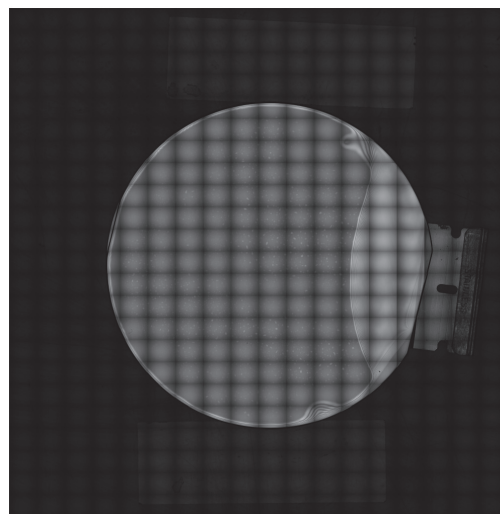


*Figure 1: Bonded wafers with speckles and blade test (Schott IR, coax stitched image).*

The Schott IR Inspector was used to inspect the quality of the bond. Lower quality bonds usually have small speckles of trapped moisture, as seen in Figure 1, which also illustrates the blade test applied to qualitatively assess the strength of the bond. Dust trapped between the wafers when bonding can be seen in Figure 2 due to the fringe pattern created around it. Finally, Figure 3 shows the good bonding results we achieved with minimal speckles and fringes.

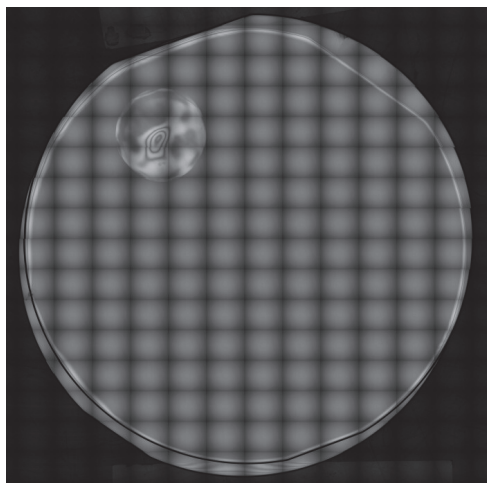


*Figure 2: Bonded wafers with speckles and blade test (Schott IR, coax stitched image).*

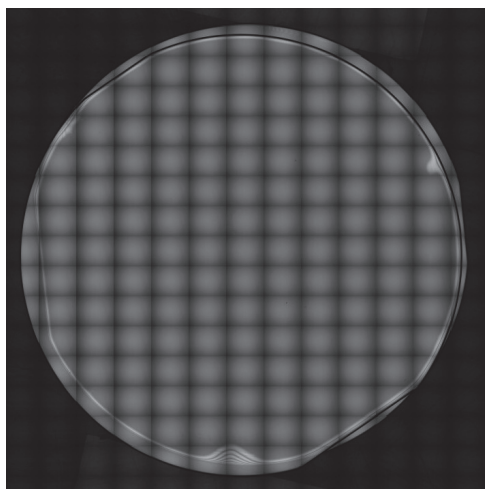


*Figure 3: Bonded wafers with no speckles/fringes (Schott IR, coax stitched image).*

## Conclusions and Future Steps:

A simple process for bonding Silicon wafers was successfully developed using tools at the Cornell NanoScale Facility. Future steps include reducing the SB8e bonding temperature down to room temperature, which could reduce bonding time as it avoids a slow cooldown step in the bonder recipe.

## References:

- [1] H Moriceau et al 2010 Adv. Nat. Sci: Nanosci. Nanotechnol. 1 043004.
- [2] Maszara, W. P., Jiang, B. L., Yamada, A., Rozgonyi, G. A., Baumgart, H., & De Kock, A. J. R. (1991). Role of surface morphology in wafer bonding. Journal of Applied Physics, 69(1), 257-260. doi:10.1063/1.347760.
- [3] U. Gösele, Q.-Y. Tong. 1998. SEMICONDUCTOR WAFER BONDING. Annual Review of Materials Research 28:215-241. <https://doi.org/10.1146/annurev.matsci.28.1.215>.