

Sensing SiGe-related Superconductor and Dielectric Material Microwave Loss via Flip Chip

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Primary CNF Tools Used: Heidelberg MLA 150 Maskless Aligner, DWL2000, PT770, ABM contact aligner, SC4500 Even-Hour Evaporator, AJA-1, DISCO dicing saw, Oxford 81, RTA

Abstract:

We developed a flip-chip-based technique that can probe the loss tangent of the target dielectric material, or the complex conductance and surface oxide loss tangent of the target superconductor thin film. We remark that this procedure is fabrication-free for the target material; thus, it can extract the intrinsic microwave loss. This approach establishes a fast-turnaround benchmarking protocol for novel materials, where loss is not accessible via conventional on-chip resonator methods. Ge/SiGe heterostructures are essential to hybrid semiconductor-superconductor devices, such as the Andreev spin qubit—a leading prospective platform for scalable quantum computing. High microwave loss in SiGe-related dielectric materials and contact superconductors remains a major bottleneck. We applied the flip-chip-based technique to study the source and potential mitigation methods in a series of SiGe-related materials.

Summary of Research:

Sensor fabrication:

The sensor fabrication includes SU-8 patterning and resonator defining. To sense the loss of the target film, the sensor must be a few microns away from the target film, with an uncertainty less than half a micron. In this project, we use 4 μm SU-8 pillars, with the whole patterning flow achieved within CNF. The SU-8 pillars are defined on niobium or tantalum thin films, where we further pattern high-quality-factor superconducting resonators. A quick optical microscope and profilometer check is performed to ensure the height and location of SU-8 pillars are within tolerance.

Target chip preparation:

The target film involved in this study includes Nb films (for benchmarking the baseline performance), SiGe-related dielectric materials, and superconductor thin films. We diced the SiGe heterostructures into a size that fits the flip-chip sensor. They underwent different treatments, such as oxygen etch to remove the quantum well (QW), HF treatment to deplete the QW, and (niobium) platinum deposition and annealing to form a (Nb)PtSiGe alloy.

Measurement:

The target dielectric materials and superconductor thin films are flipped onto the sensor and cooled down in cryostats. We measure the quality factor of the sensing resonators and analyze the performance of individual target chips accordingly.

Conclusions and Future Steps:

We demonstrated a flip-chip-based loss sensing scheme and applied it on a Ge/SiGe material series. In the coming months, we will use the sensing scheme to study multiple novel materials.

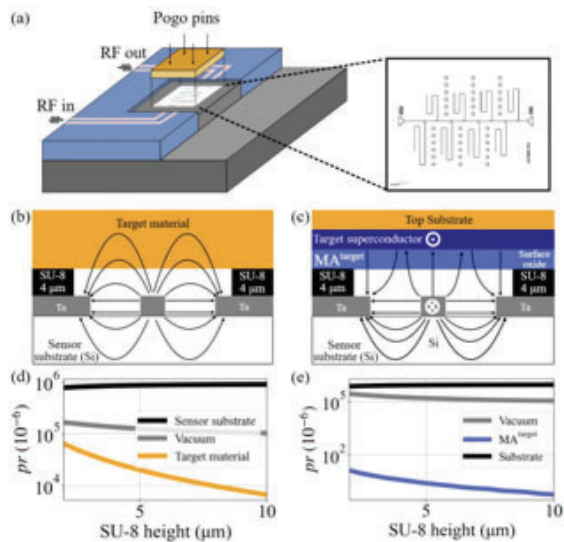


Figure 1: a) Schematic of the flip-chip-based sensor. b) Dielectric material sensing scheme. c) Superconductor thin film sensing scheme. d) Participation ratio of the dielectric target material versus SU-8 pillar height. e) Participation ratio of the target superconducting thin film surface oxide versus SU-8 pillar height.

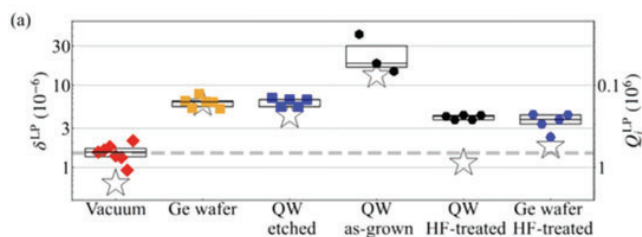


Figure 2: Boxplot of low power ($\langle n \rangle < 10$) intrinsic loss (dots) and high power ($\langle n \rangle > 10^6$) intrinsic loss (stars) for dielectric materials measured by the flip-chip-based sensor.