

Characterization of Silicon Carbide Wafers

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Abstract:

This project focused on characterizing silicon carbide (SiC) thin films deposited using low pressure chemical vapor deposition (LPCVD). The films were grown from a mixture of dichlorosilane (DCS) and acetylene (C_2H_2) gas, with hydrogen gas as the carrier gas aiding deposition, at two deposition temperatures: 800°C and 850°C. To help isolate the electrical properties of the SiC layer itself, two types of substrates were used—plain silicon wafers and silicon wafers with a deposited layer of silicon oxide. All wafers were cleaned using a standard MOS process and loaded into the A4 SiC furnace for deposition, where the ratio of DCS to acetylene was systematically varied. After deposition, the films were analyzed for thickness, refractive index, intrinsic stress, and resistivity. A noticeable drop in stress or refractive index at certain gas ratios suggested a potential change in film crystalline structure. In the final phase, ammonia (NH_3) was introduced during deposition to explore in-situ doping. Some of these doped films showed unexpectedly low stress and very high conductivity. One particular sample could not be accurately modeled using standard optical fitting tools, suggesting an unusual film structure or electronic behavior. While more work is needed, these results point toward new ways to engineer SiC films with customized electrical and mechanical properties.

Summary of Research:

This project focused on the low-pressure chemical vapor deposition (LPCVD) of silicon carbide (SiC) thin films using dichlorosilane (DCS) and acetylene (C_2H_2) gas. This work aimed to investigate the effects of deposition conditions—specifically gas ratios and temperature—on film characteristics such as thickness, refractive index, stress, and resistivity, with the broader goal of tailoring SiC films properties for potential semiconductor applications. A secondary goal was to explore the effect of ammonia (NH_3) doping on electrical and mechanical properties. The wafers used for deposition included both

bare silicon wafers and silicon wafers with deposited silicon oxide layers. The oxide-coated wafers served to isolate the electrical properties of the SiC film by minimizing current leakage into the substrate. Prior to deposition, all wafers underwent a cleaning sequence beginning with a sodium hydroxide (NaOH) base bath, followed by a rinse, then an acid bath using hydrochloric acid (HCl), and a final rinse until the surface resistivity reached approximately 16 $M\Omega\cdot cm$. These wafers were then spun dry and ready for depositions. This surface preparation ensured minimal contamination and enabled consistent film growth.

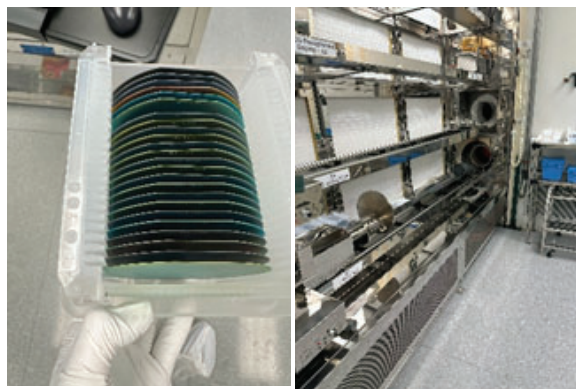


Figure 1: The picture on the right shows the furnace that was used for the deposition process. The picture on the left shows the resulted wafers that were deposited. As you can see the color of the wafers are an indicator of the thin film and this color may vary depending on the deposition conditions.

Deposition was carried out in the A4 SiC furnace under low-pressure conditions. The precursor gases—200 sccm of DCS and 50 sccm of acetylene had varying ratios where the DCS was kept at 31% max sccm while the acetylene ranged from 38% - 22% max sccm, while hydrogen was introduced as a helping gas. The hydrogen flow was found to be essential for achieving uniform films; wafers processed without it displayed black spots and non-uniform coverage. Depositions were performed at two temperatures: 800 °C and 850 °C. At 850 °C, deposition time was held around 70 minutes, while at 800 °C the process time was extended to approximately

140 minutes. These times were chosen to target a final film thickness of about 130 nm. Pressure within the furnace was actively controlled through a series of automated sequences including purging, pump-down, leak checking, and venting.

After deposition, multiple characterization techniques were used to assess the films. The RC Woollam ellipsometer was first used to measure the thickness and refractive index from the reflective surface of the wafer using a SiC optical model. The Filmetrics F50 tool was used to evaluate the thickness uniformity across the wafer surface. For stress analysis, the wafer backside was etched using the Oxford 82 system with a $\text{CF}_4/\text{O}_2/\text{Ar}$ gas mixture to expose the front-side curvature. The curvature was then measured using the Flexus tool to calculate intrinsic film stress. Finally, the electrical resistivity of the SiC layers was measured using the Filmetrics R50 system, particularly on the oxide-coated wafers to ensure that the readings were specific to the film itself.

Across both the 800 °C and 850 °C deposition conditions, the silicon carbide thin films demonstrated consistent deposition rates, with no significant fluctuations observed as the gas flow ratio between dichlorosilane (DCS) and acetylene (C_2H_2) was varied. The refractive index of the deposited films remained relatively stable, ranging from 2.7 to 2.9 throughout all runs. In contrast, the resistivity of the films showed a clear downward trend as the DCS-to-acetylene ratio increased, indicating a correlation between gas ratio and film conductivity. Similarly, film stress exhibited a decreasing trend with increasing gas flow ratio at both temperatures. These trends were consistently observed across both sets of wafers and suggest reproducible control of key film properties through process parameter variation. These graphs are shown collectively in Figure 2.

In the doping experiment, ammonia (NH_3) gas was introduced in the deposition process at varying flow rates to explore its effect on the properties of the silicon carbide thin films. Across both 800 °C and 850 °C deposition temperatures, specific NH_3 gas flow settings resulted in films that exhibited high conductivity. At a deposition temperature of 800 °C, a flow rate of 20% max sccm resulted in a film that was highly conductive, as confirmed through resistivity measurements using the Filmetrics R50. Similarly, at 850 °C, a flow rate of 60% max sccm produced a film with high conductivity. These points of interest were repeated to confirm the observed results, and in each case, the outcome remained consistent. However, under these particular doping conditions, the RC Woollam ellipsometer was unable to return a valid model fit or measure the thickness of the

films. This in turn resulted in no stress, refractive index, and deposition rate measurements for these wafers. Despite the incomplete optical characterization, the electrical measurements potentially indicate that NH_3 doping successfully altered the electronic properties of the silicon carbide films in certain cases.

Conclusions and Future Steps:

In conclusion this characterization demonstrates that the properties of SiC wafers can be tuned depending on gas ratios, temperatures and even external doping. As the acetylene gas concentration got lower, stress and resistivity also dropped. The introduction of ammonia gas can potentially lead to a more conductive wafer. Future work could focus on specific structural microscopy as the RC Woolam was not able to perfectly characterize some wafers. Other future work could also be in the introduction of ammonia and optimizing the conditions for the best conductivity.

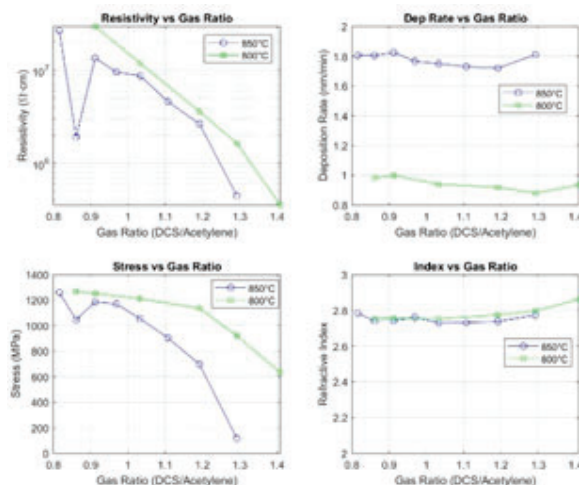


Figure 2: The graphs and their trends are shown above where blue represents 850 °C and green represents 800 °C.

Acknowledgements:

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Baseline Etch Processes: Evaluating Etching and Stripping Tools

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Primary CNF Tools Used: Oxford 81, Oxford 82, PT740, FilMetrics F50, P-7 Profilometer

Abstract:

Reactive Ion Etching is a technique that can achieve highly anisotropic etches, as well as high selectivity. Etching is performed by high energy ions as well as reactive species that interact with the surface, with an etch rate dependent on the recipe and the material being etched. Certain tools in the cleanroom, such as the PT740, Oxford 81, Oxford 82, and Glen 1000 all have stated etch rates for certain recipes. However, over time, these rates have changed from when the measurements were originally taken, meaning the manuals may no longer be accurate. The goal of this project is to measure the current etch rates of these machines across many recipes and materials to update the manuals, ensuring that future users will be able to more precisely etch their samples.

Summary of Research:

When measuring etch rates on the PT740, Oxford 81, and Oxford 82 tools, recipes stated in their respective manuals were used. Measurements of the samples before and after etching were performed by the FilMetrics F50 optical metrology tool, allowing for the characterization of etch rates across the sample. Silicon oxide wafers were deposited using 4 different PECVD methods; high rate, low rate, HDP, and TEOS deposition. Silicon Nitride wafers (figure 1) were produced with PECVD, LPCVD, HDP-CVD, as well as with the NIT N=2 recipe on the PT Takachi HDP-CVD. Carbide wafers were made by LPCVD. All aforementioned wafers were produced by Aaron Windsor. The Glen 1000 oxygen plasma tool was also characterized alongside the RIE machines. Three different resists were measured: Shipley 1813, nLof Az 2020, and SPR220-3.0. These were characterized using the RIE configuration of the Glen 1000 (figure 4), with etch rates measured using the P-7 profilometer. The final characterization that was performed was BARC (Bottom Anti-Reflective Coating) strip times. With a

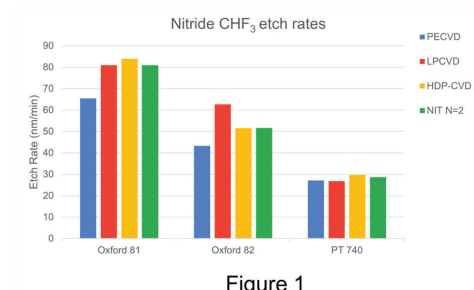


Figure 1: Etch rates over 3 tools and 4 deposition methods of silicon nitride, showing trend that the Oxford 81 is the fastest, followed by the Oxford 82, then the PT740.

ARC removal tool:	Wattage	Minutes:
Glen rack A	500W	5
Glen rack B	500W	1
Glen rack C	500W	4
Glen rack A	400W	5
Glen rack B	400W	1
Glen rack C	400W	6
Anatech	300W	3
Yes asher	100W	14
Yes ecoclean asher	3000W	1

Figure 2

Figure 2: Time to remove ARC layer over different tools.

thin layer of BARC, incremental 1-minute runs on different machines were performed, until the coating was no longer measurable on the wafer. Two machines were able to remove the layer in under a minute; the Glen 1000 rack B (either 400 or 500 W), as well as the YES Ecoclean Asher using the recipe "0resist_strip_1min" (figure 2).

Etch/strip rates:

When comparing the measured etch rates with the etch rates stated in the manuals, two machines have changed considerably since the last time they were characterized.

The Oxford 82 recipe " CHF_3 / O_2 oxide etch" was stated to have an etch rate of 43 nm/min, however, the measured etch rate is only around 25 nm/min. The " CF_4 / O_2 oxide etch" also has decreased over time, as the stated etch rate is 42 nm/min, while the measured etch rate is

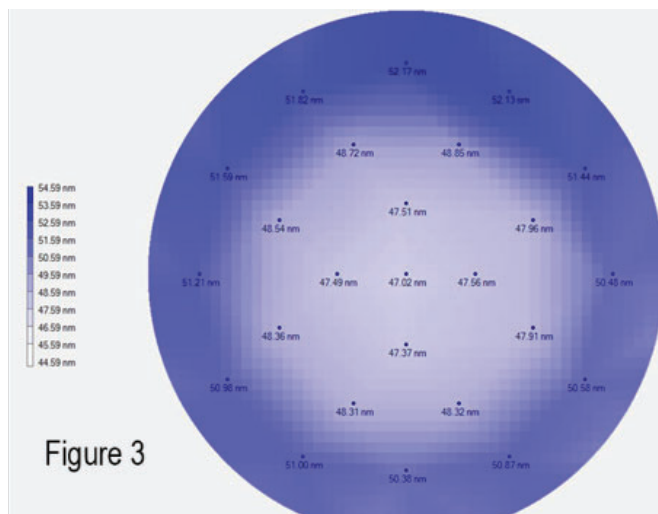


Figure 3: Difference map of before and after an etch with the PT740, showing a higher etch rate along the edge of the wafer.

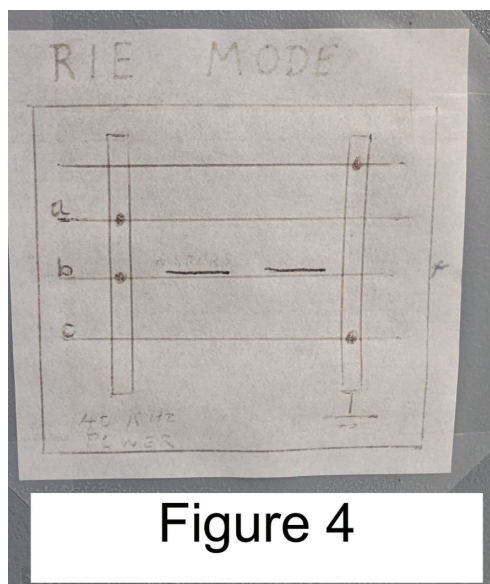


Figure 4: Design showing the configuration of the Glen 1000 during testing, with 1st and 4th rack being grounded, and the 2nd and 3rd rack attached to power.

closer to 21 nm/min. The Glen 1000, has significantly changed since the last characterization, which was taken around 2003. The old stated values for racks A, B, and C are respectively; 300nm/10min, 730nm/10 min, and 280nm/10 min. The current measured values are 92 nm/10 min, 410 nm/10 min, and 41 nm/10 min. The PT740 manual had one stated recipe that did not match the measured rate, that being the ' $\text{CHF}_3 / \text{O}_2$ nitride etch LSN', with the stated value being 19 nm/min, and the measured value 27 nm/min. However, this etch rate was characterized recently, and it is suspected that the etch rates of the PT740 vary due to other uncontrolled factors, so further testing would be required to definitively state whether this recipe needs to be updated.

Uniformity:

Tests were run on the RIE machines using 100mm wafers. The two Oxford 80 tools have similarly uniform etches, with a uniformity of around $\pm 2.5\text{-}3\%$. The Oxford 81 appears to etch slightly faster in the center than the outside, with the Oxford 82 being the opposite. With the PT740, however, it is clearly visible that the outside of the wafer etches with the highest rate, with the outside of the wafer (10mm from the edge) etching around 10% faster than the middle (figure 3). This machine has a uniformity across the wafer of around $\pm 5\%$.

Conclusions and Future Steps:

When etching Silicon compounds, the tool with the highest etch rate is the Oxford 81, followed by the Oxford 82 then the PT740. The fact that the two Oxford tools have differing etch rates is surprising, given that they are two identical instruments. The reason for this discrepancy is unclear, and determining and correcting the cause of this difference is a possible area for future work. Using this new data the recipes for the Oxford 82 stated in this report should be updated, as well as all the numbers on the Glen 1000. BARC stripping can now be suggested for some users with material restrictions to be done in the Glen 1000 rack B or the YES Ecoclean Asher could be used.

Acknowledgements:

Special thanks to Aaron Windsor and Lynn Rathbun for enabling me to have this amazing hands-on experience, as well as providing consistent support throughout this summer. I also would like to thank the rest of the Cornell NanoScale Science and Technology Facility for allowing me to perform this research.

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Determining Out-of-Plane Structure via Electron Diffraction

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Abstract:

In situ studies of phase transitions in materials are essential to understanding structure evolution, and thus engineering for novel or advanced applications [1]. This is especially true in battery materials where dramatic, intercalation-induced phase transitions impact safety, reliability, and performance [2]. Scanning transmission electron microscopy (S/TEM) provides simultaneous imaging, diffraction, and spectroscopy data from a single instrument. However, in situ intercalation experiments in the TEM are uncommon and often rely on highly specialized holders [3]. Here we characterize the complete lithiation-induced phase transition in the layered van der Waals (vdW) material, lanthanum tritelluride (LaTe_3), using a standard electrical biasing holder by fabricating electrochemical cells that are liquid-free.

Throughout lithiation of the LaTe_3 flake, we observed at least two distinct phase transformations, various LaTe_3 stackings, and an expansion and subsequent relaxation of the in-plane lattice. During this experiment, several types of data were acquired: atomic resolution and low-magnification STEM imaging, electron energy loss spectroscopy (EELS), and spatially resolved diffraction using four-dimensional STEM (4D STEM). The combined analysis of these datasets reveals the morphological, electronic, chemical and structural changes of the flake during intercalation. The experimental patterns observed were replicated by multislice simulations (abTEM [5]) from different $1 \times 1 \times 3$ supercells with lithium ordering in vdW gap interstitials (Figure 2).

A later experiment includes 4D STEM data from convergent beam electron diffraction (CBED). This provides out-of-plane structure due to interactions with the higher order Laue zone (HOLZ) of the reciprocal lattice. Simulations confirm individual stackings are

distinguishable from each other and from out-of-plane disorder. CBED analysis via Hough circle transforms [6] allows us to measure out-of-plane strain.

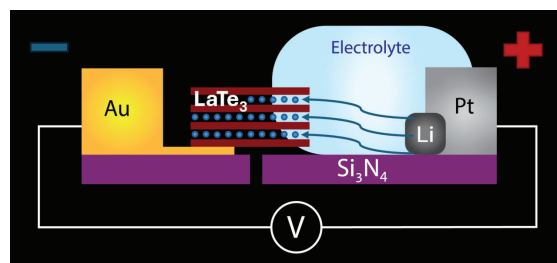


Figure 1: The all solid-state electrochemical cell, where the voltage bias controls lithium intercalation in the vdW gaps between LaTe_3 layers.

Summary of Research:

In each in situ experiment, we utilize an off-the-shelf electronic chip (e-chip) placed in a standard Protochips Fusion350 heating/biasing holder. The all solid-state electrochemical cell is displayed in Figure 1. At the start of the experiments, the LaTe_3 flake is in the pristine state, as shown in Figure 2a. EELS analysis tells us there is no detectable lithium in this phase. In the first experiment, after measuring an open circuit voltage of 2.3 V, we initiated intercalation by lowering the cathode potential to 0 V (vs Li anode). After 10 minutes, we observed an intercalation-induced new phase propagated across the flake, verified by low magnification STEM imaging. The EELS data taken 35 minutes after initiating intercalation showed an increase in intensity following the Li-K edge onset at 57 eV. Representative diffraction patterns in this phase revealed two lithiated structures with the same ordering: one maintaining the bulk stacking and one with a layer shifted by half the lattice (Figure 2b), as seen in the alignment of Te-nets across the vdW gap. 4D STEM analysis at this stage showed significant in-plane lattice expansion of approximately 1.5%.

After continuing intercalation at the 0 V cathode potential, the flake did not exhibit further significant changes. Approximately 4 hours into the experiment, we lowered the cell voltage to -9 V. By the 5.5-hour mark, we observed a second major phase transformation. The lithium-ordering superlattice disappeared (Figure 2c) and the previous in-plane lattice expansion had relaxed. Simulated diffraction of the proposed structures matches the experimental diffraction patterns from their respective lithiated phases (Figure 2). We attribute the in-plane strain relaxation to the addition of out-of-plane unit cell expansion. CBED simulations result in diffraction patterns containing HOLZ rings, whose radii we measure with Hough circle transforms. This analysis is robust to sample tilt, and the measured radius of HOLZ rings is inversely correlated with the out-of-plane strain of each stacking (Figure 3). The CBED patterns of different stackings are distinguishable from one another, which allows us to measure out-of-plane strain while preserving phase information.

We determined the optimal TEM parameters with more simulations, then ran the experiment again using scanning CBED. Preliminary analysis shows significant out-of-plane disorder in later stages of lithiation. This causes the HOLZ rings to blur, making them more challenging to measure with the Hough circle transform alone. We aim to increase the precision of our measurement method and subsequently pair it with a radial average integration technique. Currently, we are using simulations to investigate the resultant diffraction patterns caused by various types of disorder.

Conclusions and Future Steps:

In situ experiments allowed us to identify two distinct phase transformations of LaTe_3 via multimodal STEM (imaging, EELS, and 4D STEM). To enable this complete characterization in a single experiment, we developed an all solid-state electrochemical cell on a standard Si_3N_4 membrane-style TEM e-chip. We developed techniques for mapping structural information during the intercalation process, including out-of-plane stacking and unit cell expansion. We perform these measurements over large fields of view using 4D STEM. With abTEM multislice simulations, we determined optimal CBED parameters and repeated the intercalation experiment. Looking forward, we aim to improve measurement precision, further investigate out-of-plane disorder, and complete the remaining analysis of our latest dataset. Our method should enable future investigations of other intercalation materials to directly and comprehensively observe their phase transformations.

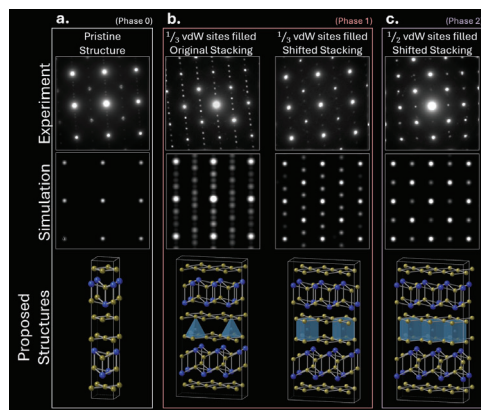


Figure 2: (a) The pristine structure, which contains no lithium, (b) the first phase transformation, where $1/3$ of the vdW sites are filled and we observe the original as well as a shifted stacking, and (c) the second phase transformation, where $1/2$ of the vdW sites are filled and we only observe shifted stacking.

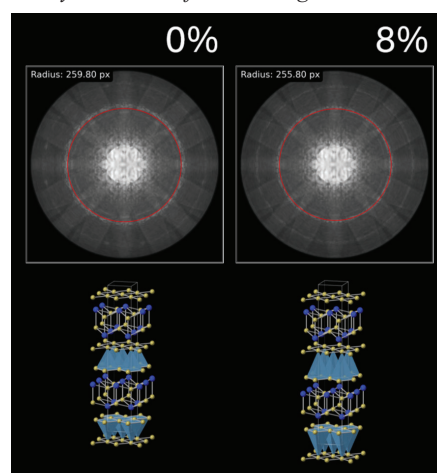


Figure 3: A demonstration of the inverse relationship between out-of-plane unit cell expansion and HOLZ ring radius.

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Silicon Interposer for Millimeter-Wave Heterogenous Integration: Doped vs. High Resistivity Substrates

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Primary CNF Tools Used: SUSS MA6-BA6 Contact Aligner, AJA Sputter Deposition, UNAXIS 770 Deep Silicon Etcher,

PlasmaTherm Versaline System, Veeco Savannah ALD, ReynoldsTech Cu ECD Hood, DC Probe Station, Microwave Small-Signal Probe Station

Abstract:

As the demand for heterogeneous-integrated RF chips increases, interposers for millimeter-wave circuits using through-silicon vias (TSVs) have become increasingly important due to their low loss and high-power capacity across a wide frequency range. For frequencies above 110 GHz, substrate-integrated waveguides (SIWs) are small enough to be integrated in Si interposers for high-power interconnects.

They can also be used to form high-quality passive devices such as filters and antennas, which have been difficult to integrate on-chip. This enables system-on-chip. In this study, we investigate the fabrication of SIWs and grounded coplanar waveguides (GCPWs) in silicon (Si) interposers with a thickness on the order of 200 μm with resistivities ranging from 10 to 1 $\text{k}\Omega\cdot\text{cm}$. Thin Si wafers were patterned and etched using the Bosch deep reactive ion etching (DRIE) process to create TSVs. The TSVs are then metallized with platinum (Pt) using atomic layer deposition (ALD) and filled with copper (Cu) using electroplating deposition. DC measurements confirm a TSV series resistance of less than 1 Ω . Small-signal millimeter-wave on-wafer measurements show that the coplanar interconnects fabricated on high-resistivity (HR, resistivity $> 1 \text{ k}\Omega\cdot\text{cm}$) Si have an insertion loss of 0.7 dB/mm at 40 GHz, an order of magnitude better

than the same coplanar interconnects fabricated on doped Si (resistivity $< 10 \Omega\cdot\text{cm}$).

Summary of Research:

Si is the most extensively used material in semiconductor

devices due to its exceptional electrical and mechanical properties, including a high dielectric constant, electrical resistivity, breakdown strength, and low loss tangent. These characteristics make it an attractive candidate for SIWs. However, its relatively low mechanical toughness and high thermal conductivity compared to materials like silicon carbide (SiC) pose challenges during processing, particularly in etching processes. Our group has previously demonstrated SiC as a viable substrate material for SIW processing. The methodology developed for SiC SIW fabrication is adapted as a proof of principle for Si SIW fabrication.

To develop a processing recipe for Si-based SIWs, we used a thinned HR Si wafer with a thickness of approximately 200 μm and resistivity greater than 1 $\text{k}\Omega\cdot\text{cm}$. Building on a similar methodology used for SiC SIWs while leveraging the more mature and faster etching processes available for Si, we began by depositing a 50 nm layer of aluminum oxide (Al_2O_3) on the wafer's backside using AJA Sputter

Deposition. Al_2O_3 was selected as the etch mask due to its excellent masking performance in the Bosch DRIE process for Si, providing a high selectivity greater than 1:1000.

The DRIE was performed using either the UNAXIS 770 Deep Silicon Etcher or the PlasmaTherm Versaline System. To ensure effective cooling during etching, the Si wafer was bonded to a sapphire carrier wafer using cool grease. The etching chemistry employed $\text{C}_4\text{F}_8/\text{SF}_6$, which react with Si to

anisotropically form vias. As shown in Figure 1, this process yielded 200 μm -deep TSVs with a diameter of 50 μm and sidewall angles ranging from 80° to 90° .

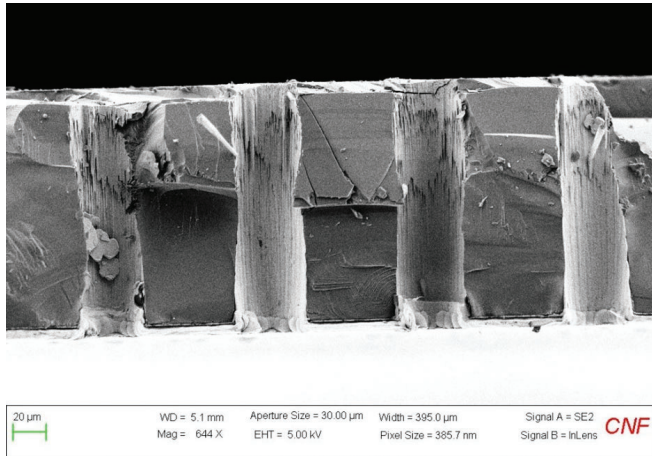


Figure 1: Cross-Sectional SEM Images of TSVs.

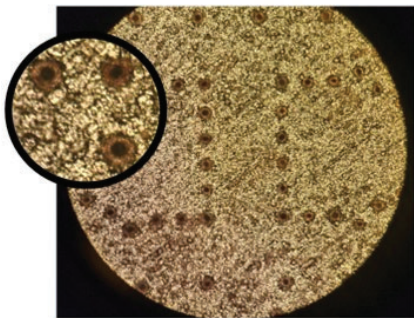


Figure 2: Top-View Optical Image of TSVs After Cu Electroplating.

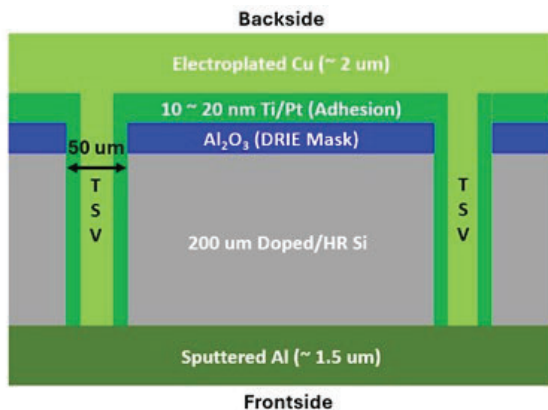


Figure 3: Schematic of Si Interposer Layout.

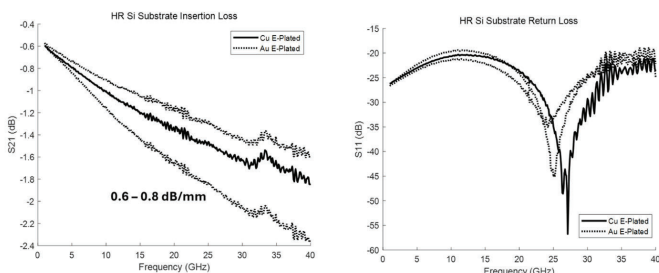


Figure 4: Measured Insertion Loss (S_{21}) and Return Loss (S_{11}) of HR Si Substrate Across 1 – 40 GHz.

After the TSVs were fully etched through, ALD was used to coat the TSV sidewalls with a Pt seed layer. Cu was then electroplated to fill the TSVs, initiating from the Pt seed layer, as illustrated in Figure 2.

Once the backside processing was completed, the front side was patterned with SIW and GCPW lines. A titanium/aluminum (Ti/Al) layer was subsequently deposited using AJA sputter deposition. The structural details and final device configurations are shown in Figure 3.

Both HR and doped Si devices were tested at the High Frequency Test Lab (HFTL) where TSV series resistance and GCPW line performance were evaluated. Using the DC probe station, I-V measurements showed that the TSV series resistance was typically below 1 Ω for both HR and doped Si substrates. RF

measurements were then conducted over 1 – 40 GHz range using the small-signal probe station, as shown in Figure 4. For HR Si, insertion loss (S_{21}) values ranged from 0.6 to 0.8 dB/mm, with return loss (S_{11}) exceeding 20 dB. In comparison, doped Si devices exhibited insertion loss of approximately 3.2 dB/mm and return loss greater than 10 dB.

Conclusions and Future Steps:

The fabrication of Si interposers focused on optimizing Bosch DRIE of thinned Si wafers and refining metallization processes to achieve uniform anisotropic etching and consistent metal filling across the wafer. Measurements comparing HR and doped Si substrates revealed that HR Si exhibits insertion loss an order of magnitude lower than that of doped Si, highlighting its potential as a promising substrate material for millimeter-wave applications. Looking ahead, with updated tools and improved techniques for etching and metallization, fully metal-filled TSVs are expected to achieve insertion losses below 0.5 dB/mm at frequencies up to 220 GHz, utilizing the 220 GHz single-sweep probe station at HFTL.

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Alpha-Tantalum Thin Film Deposition on Pure Silicon Wafers with the Angstrom-Q

CNF Summer Student: Porter Rowbotham

Student Affiliation: Mechanical Engineering, Rochester Institute of Technology

Summer Program(s): Summer 2025 CNF NORDTECH Intern

Mentor(s): Aaron Windsor - Thin Film Process Engineer, CNF

Primary Source(s) of Research Funding: NORDTECH

Contact: pjr4887@rit.edu

Research Group Website: <https://www.nordtechub.org>

Primary CNF Tool Used: Angstrom-Q, Filmetrics R50, Zeiss Ultra SEM

Abstract:

Material choice in superconducting quantum circuits can greatly impact device coherence and losses. Recently, Tantalum thin films have shown great potential for transmon qubit fabrication, boasting high resonating times and high quality[1]. Tantalum's α crystal phase is especially important as it boasts a superconducting critical temperature of 4.2°K. Recent studies have shown that using a heated substrate can enable α -Tantalum thin film deposition [2,3,4]. The Cornell Nanoscale Facility recently introduced a new quantum-oriented electron beam evaporation tool with the capabilities to deposit these films, the Angstrom-Q. The project for this summer is to find the transition temperature where α -Tantalum can be deposited.

Summary of Research:

All samples for this project are deposited on 100mm undoped silicon wafers. All Tantalum depositions are completed at 1Å/s to a final thickness of 500Å.

Deposition Temperatures:

The temperature at which deposition takes place across different tools for α -Tantalum deposition can vary greatly based on the temperature measurement or deposition method. Sputtering an α -tantalum film may require a higher heat than evaporation as evaporation's particles carry heat onto the surface of the substrate. With studies showing α -Tantalum growth at 350°C [2], 400-500°C[3], and 600-650°C[4]. With this data, we chose to do a baseline run at room temperature, and then start at 350°C, moving at 50°C increments until the transition temperature is found, then move to 10°C increments.

Wafer cleaning:

One of the most important steps in creating a high quality α -Ta film is the cleaning. The wafers are RCA cleaned at the CNF MOS tanks, followed by a 60s bath in 20:1 HF

to remove any surface oxides. This process remained until a water-streaked, highly non-uniform film began to appear at deposition temperatures above 425°C. We suspected that the HF bath in the MOS bath may be contaminated, or that the wafer was being oxidized by spending too long being rinsed in DI water. To correct this, we switched to removing the surface oxides by using 10:1 HF for 60s and 30s dip in DI water by hand. Additionally, it was found that the samples should spend less than one hour between the finish of the MOS clean and being processed.

Heated Deposition:

Once the wafer is fully cleaned and has its surface oxides stripped, it is placed in the Angstrom-Q load lock and put under vacuum. This is done in less than ten minutes to avoid the re-growth of surface oxides. Once in the machine, the wafer is heated to the desired deposition temperature, and then held at that temperature for 60 minutes to ensure even heating across the substrate. The wafer and carrier are allowed to cool and removed once reaching a temperature lower than 100°C.

Resistivity:

One convenient method to determine the crystallinity of a tantalum film is the film's resistivity. The room temperature resistivity of β -Ta is 150-200 $\mu\Omega$ -cm and the resistivity of α -Ta is 15-20 $\mu\Omega$ -cm [3]. We used the Filmetrics R50 four point probe to measure the sheet resistance of the film, then multiplied the sheet resistance by the thickness of the film to find the resistivity of the samples (Figure 1).

X-Ray Diffraction:

X-Ray Diffraction (XRD) scans were completed on all of the samples using the Rigaku SmartLab X-ray Diffractometer at the Cornell Center for Materials Research by Lingda Kong. Matching known scan peaks to our experimental runs shows what crystalline phase the sample is (Figure 2).

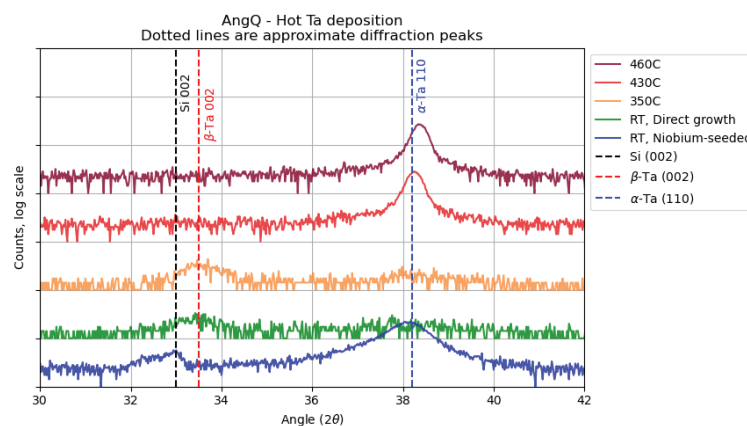
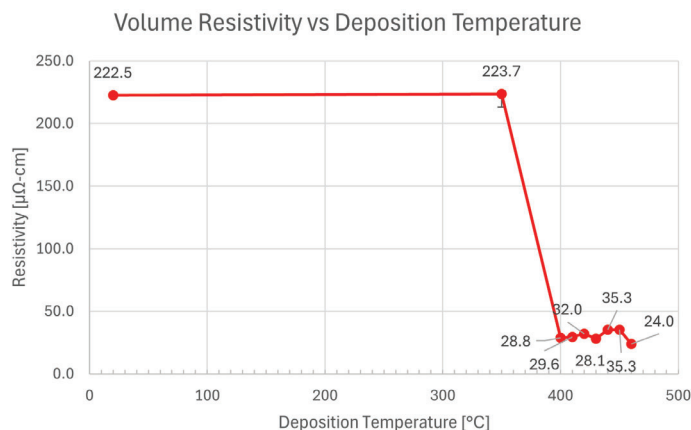


Figure 1 (Left): Volume Resistivity of Samples vs. their Deposition Temperature. Figure 2 (Right): X-Ray Diffraction Scans of Several Samples

Seed Layers:

A popular method for growing an α -Tantalum film is to use a thin layer of another material to avoid Tantalum-Silicon interactions and promote the correct crystalline phase. We did one Niobium seeded Tantalum deposition with 5Å of Niobium and 50Å of Tantalum, both deposited at 1Å/s at room temperature. The niobium seed layer sample had a RT resistivity of 60.8μΩ-cm. XRD scanning showed a peak around the α -Tantalum region without a peak in the α -Tantalum range (Figure 2).

Conclusions and Future Steps:

With this data, we can conclude that mostly pure α -Tantalum depositions on pristine silicon wafers at temperatures above 400°C, and that the transition temperature may lay in the 350-450°C range. Niobium seeded tantalum deposition shows α -Tantalum results at room temperature. Further depositions could be used to find the exact temperature range to form pure α -Tantalum. Additionally, films should be investigated to see if Tantalum Silicides (TaSi₂) are being formed. Once completed, quantum computing components could be fabricated.

Acknowledgements:

Special thanks to NORDTECH and the Cornell Nanoscale Facility for funding and hosting this internship. Thanks to my CNF staff mentor Aaron Windsor, and CNF staff Shilling Du for their help and guidance. Thanks to Fatemi Lab, and its members Lingda Kong and Tathagata Banerjee for all of their helpful insights and guidance.

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Characterization of Silicon Oxide Etching with Low Global Warming Potential Hydroolefin

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Summer Program(s): 2025 Cornell NanoScale Facility Research Experience for Undergraduates (CNF REU) Program

Mentor(s): Jeremy Clark, Cornell NanoScale Science and Technology Facility, Cornell University

Primary Source(s) of Research Funding: National Science Foundation under Grant No. NNCI-2025233,

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Summer Program Website(s): <https://cnf.cornell.edu/education/reu>

Primary CNF Tools Used: Gamma Automatic Coat-Develop Tool, ASML PAS 5500/300C DUV Wafer Stepper, P7 Profilometer, Zeiss Ultra SEM, Zeiss Supra SEM, Oxford 82 Etcher, Oxford 100 ICP-RIE Dielectric Etcher, YES EcoClean Asher, and Thermal Oxidation Furnace

Abstract:

The semiconductor industry utilizes hydrofluorocarbons (HFCs) for many different etch processes. HFCs, however, have high global warming potential (GWP). The American Innovation and Manufacturing Act of 2020 enabled the U.S. EPA to scale down the use and production of HFCs. Hydroolefins (HFOs), originally created by the refrigerant industry to reduce reliance on HFCs, show promise as an etch gas in reactively ion etched (RIE) anisotropic etching. This work explores the optimal etch conditions of

HFO-1234ze(E), or $C_3H_2F_4$ on the Oxford PlasmaLab 100 Inductively Coupled Plasma Reactive Ion Etcher. Etch rates remained similar to other oxide etch chemistries, though RIE lag remains a concern, especially with higher concentrations of $C_3H_2F_4$ in the plasma. Deposition and delamination occurred occasionally in the process of characterization, when $C_3H_2F_4$ concentration was too high or the DC voltage bias became too low. $C_3H_2F_4$ holds promise for regular use as a silicon oxide etch gas with more characterization and process research.

Summary of Research:

Silicon oxide is a common etch material in the semiconductor industry and is often etched with hydrofluorocarbons (HFCs) for their versatility and availability¹. Though HFCs are not ozone-depleting, they have high global warming potentials (GWP), contributing to global warming in the atmosphere. The AIM Act of 2020 allowed the EPA to begin the scale down in use and production of HFCs, creating a need in the semiconductor industry for new silicon oxide etch gases. HFO-1234ze(E), or $C_3H_2F_4$ has shown potential in silicon etching but it has not been characterized definitively^{1,2}. A broad analysis was thus conducted to test the etch rate, selectivity, sidewall angle, and RIElag

of various etch recipes of $C_3H_2F_4$. RIElag is the effect of smaller features etching at a slower rate to larger features. It can be reduced by altering the properties of an etch plasma. The Oxford PlasmaLab 100 was used to characterize $C_3H_2F_4$ since, as an ICP etcher, it allowed the individual control of multiple different parameters, controlling the plasma both chemically and physically. Patterned and blank silicon oxide wafers were tested on the Oxford 100 over the course of the experiments.

About 1 micron of silicon oxide grown on Silicon test wafers in a wet oxide furnace. Most wafers were patterned using the Gamma Automatic Coat-Develop Tool, though some wafers were hand-spun, replicating the Gamma processes. BARC was spun on wafers for 30 seconds at 2400 rpm, before a 60-second, 205° bake. Next, UV210-0.6 photoresist was spun at 2900 rpm for 30 seconds, with a 60-second, 135° bake. The wafers were patterned using the ASML PAS 5500/300C DUV Wafer Stepper. Two patterns were used, a standard edge-clear pattern and the ALE Test Mask for RIElag that has trenches of varying width, from 5 micron to 300 nm, with large additional corner features. Finally, the wafers were developed with a 135° bake for 90 seconds, before a 60-second 724MIF develop.

Every patterned wafer had an BARC removal with a 1-minute, 45-second ARC etch on the Oxford 82. After, step height of the large corner features was measured with the P7 Profilometer using a shortened version of a pre-existing sequence, testing 10 different corners. Each wafer was etched in the Oxford 100. Prior to each etch, the Oxford 100 was cleaned and seasoned for 2 minutes with either a bare silicon wafer or a blank silicon oxide wafer, to test for deposition. After etching in the Oxford 100, the P7 sequence was run again before the wafer was cleaned with a 5-minute photoresist-strip recipe on the YES EcoClean Asher. A last step height measurement was taken with the P7 sequence. Each relevant wafer's

depth and sidewall angle of the largest and smallest feature was measured using the Zeiss SEM Ultra. Wafers with deposition etches were measured for the height of the deposition. Wafers that delaminated or etched less than 40 nm of silicon oxide were not measured on the SEM.

Table 1: Initial Characterization Etches and Results.

Etch Recipe and Time	Oxide Etch Rate (nm/min)	Selectivity Oxide:Resist	Avg. Sidewall Angle	RIELAG
C ₃ H ₂ F ₄ High He (2 min)	217	6.3	95	0.72
CH ₂ F ₂ /High He (116 sec)	156	2.8	98	0.80
CHF ₃ /O ₂ Oxide (2 min)	168	1.7	93	0.83
C ₂ F ₆ /High He Oxide (2 min)	261	1.4	135	0.98
5 sccm CH ₂ F ₂ , 40 sccm C ₂ F ₆ , 3 sccm C ₃ F ₈ , 20 sccm Ar (2 min)	231	1.9	127	0.98

Table 2: Final Experiment Parameters

Parameter	Min	Max
ICP (W)	1500	2500
RIE (W)	40	80
Pressure mTorr	4	8
Gas Ring	Off	On
C ₃ H ₂ F ₄ (sccm)	10	30
He (sccm)	20	90
Ar (sccm)	0	50

Table 1 (Left): The five etches used and their resulting etch rates.

Table 2 (Right): Final Experiment Parameters.

A round of characterization etches compared the capabilities of the given C₃H₂F₄ recipe to that of other common silicon oxide etch recipes. Table 1 shows the five etches used and their resulting etch rate, selectivity, and RIElag. RIElag was calculated by the ratio of the smallest feature's depth to the largest feature's depth; the closer the value to 1, the less lag in etch rate of smaller features. The results confirmed that C₃H₂F₄ held potential as a silicon oxide etch gas. It had similar results in etch rate and sidewall angle, which was measured as the inside angle from the etched depth to the sidewall. Selectivity was improved from the other etches, but RIElag was worse. Thus, RIElag was the focused goal of continuing experimentation with additional goals of staying on target with selectivity, etch rates, and sidewall angle.

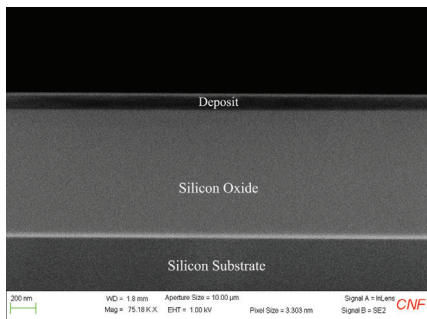


Figure 1: Deposition wafer.

Next, an experiment was designed using the JMP DOE software to find the optimal way to characterize multiple parameters within the etch recipe in a minimum number of wafers. The initial parameters used were the chamber pressure, the RF power, the ICP power, the usage of the gas ring to dispense C₃H₂F₄, and the concentration of C₃H₂F₄ to Helium. The experiment, however, immediately resulted in much deposition instead of etching. The experiment was ended to allow for more characterization attempts with blank silicon

oxide wafers to determine better value ranges for each parameter. Many of these characterization attempts resulted in deposition, with some wafers having nearly 400 nm of C₂F₄ deposited in 2 minutes, and delamination, slowly approaching more appropriate value ranges. A deposition wafer is shown in Figure 1. From this characterization, it was determined that high concentrations of C₃H₂F₄ and low DC voltage bias were likely causes of deposition.

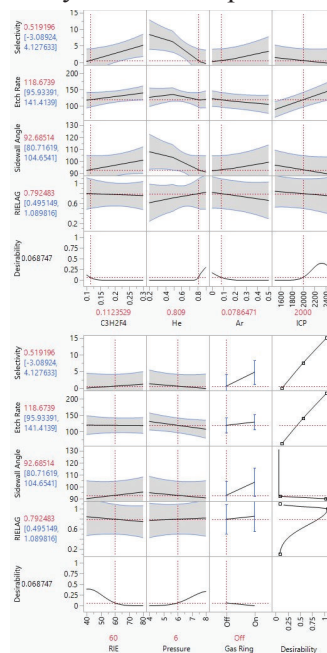


Figure 2: Results from Argon addition.

target with other silicon oxide etch recipes. RIElag varied with only a few recipes improving from the original's capability. From the results, it is evidenced that lower concentrations of C₃H₂F₄ with higher concentrations of Helium result in the best etch rate, RIElag, and sidewall angle. It should also be noted that there is a connection between increased RIE power and decreased RIElag, which would be a site for future research to build on. Though the results of this study were broad, they support further research and characterization on C₃H₂F₄ for future use across the semiconductor industry as a low GWP silicon oxide etch gas.

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Characterization of the Heidelberg MLA 150

CNF Summer Student: Jason Xu
Student Affiliation:

Summer Program(s): 2025 Summer CNF NORDTECH Intern

Mentor(s): Giovanni Sartorello, Cornell NanoScale Science and Technology Facility, Cornell University

Primary Source(s) of Research Funding: National Science Foundation under Grant No. NNCI-2025233, The Northeast Regional Defense Technology Hub

Contact: tjp83@cornell.edu, jasonxu810@gmail.com

Research Group Website: <https://www.nordtechub.org>

Primary CNF Tools Used: AJA Q, AJA Q2, Filmetrics R50, Flexus Film Stress Measurement, Hamatech Hot Piranha, P-7 Profilometer, Veeco Icon AFM

Abstract:

This research on the Heidelberg MLA 150 focuses on three key areas to optimize its performance: Dose and Defocus Tests, Alignment Tests, and Resist Characterization. The Dose and Defocus Tests aim to identify the ideal energy (dose) and laser optics position (defocus) for machine operation, with particular emphasis on regularly monitoring and correcting defocus drift caused by software malfunctions or stage crashes. Alignment Tests verify the functionality of the machine's internal alignment system by assessing the precision with which the laser writes complimentary patterns based on camera-read substrate patterns. Any misalignments are quantified, and correction factors are calculated. Finally, Resist Characterization involves empirically determining optimal exposure doses for various resists, populating a database that future users can access for efficient and accurate material processing.

Summary of Research:

My research on the Heidelberg MLA 150 has been focused around three main tests/areas: Dose and Defocus Tests, Alignment Test, and Resist Characterization. The purpose of Dose and Defocus Tests is to determine the optimal Dose and Defocus for the machine to operate. Dose is a measure of the nominal energy used to expose the substrate, while defocus is a measure of the position of the machine's laser optics. We can determine the most optimal combination of dose and defocus by exposing test patterns at various dose and defocuses and reading the resolutions of the tests. Attention is focused on the Defocus, as it is much more likely to drift due to software malfunctions and stage crashes. As a result of these crashes, Dose and Defocus Tests must be carried out regularly to ensure that the optimal dose and defocus values are known. The purpose of Alignment Tests is to

ensure that the alignment system within the machine is working properly, by loading a substrate that contains patterns spread around that may be read by a camera within the machine. The camera sends the information to the alignment system, which relays to the laser where it believes the substrate and staging is, which then writes a complimentary pattern to the original pattern on the substrate. We read how well the two patterns fit together, which tells us whether the alignment system is working properly [2]. Oftentimes, the alignment is not perfect, and we are able to calculate a correction factor to input into the machine by reading the offsets of the patterns. The rest of the time on the Heidelberg MLA 150 was spent on Resist Characterization. By testing a large range of doses on various resists, we were able to determine the optimal doses for many resists that we add to a database that future users may access and quickly determine the optimal dose to expose at.

Conclusions and Future Steps:

Dose and Defocus Tests and Alignment Tests must be regularly conducted due to stage crashes and other natural shifts. These ensure that users are always exposing at the most optimal dose and defocus and that the alignment system is working properly. Besides these tests, the database for Resist Characterization may always be added upon, and future time should be spent characterizing a larger selection of resists.

Acknowledgements:

Special thanks go out to Giovanni Sartorello for his support and mentorship throughout this internship. I would also like to acknowledge the Cornell NanoScale Facility for hosting this experience. This work was funded by a grant from NORDTECH.

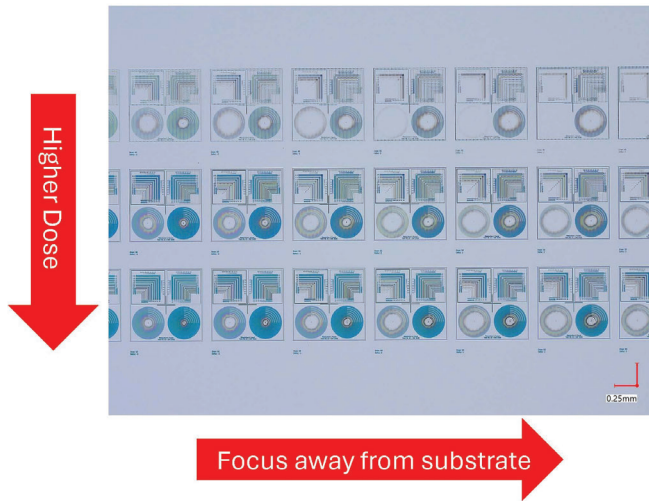


Figure 1: Dose and Defocus Test on a Wafer Coated in S1805.

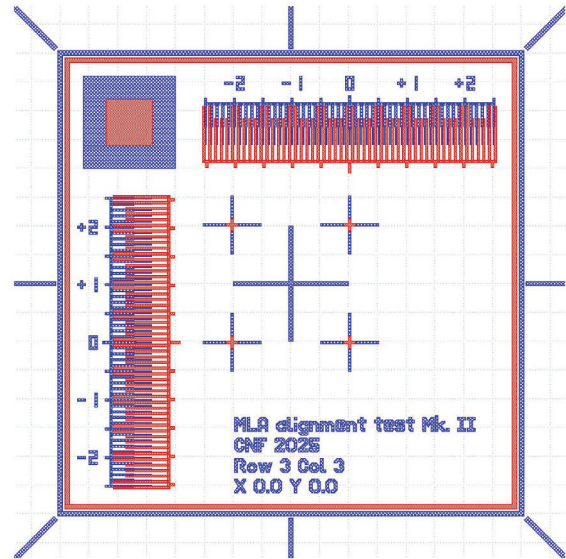


Figure 2: Alignment Test gds File.

Redistribution Layers on Glass Wafers

CNF Project Number: 3018-22

Principal Investigator(s): Shelby Nelson

User(s): Nick Stucchi

Affiliation(s): Mosaic Microsystems, LLC

Primary Source(s) of Research Funding: U.S. Department of Defense (DOD), Customer Contracts

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Research Group Website: Website: <https://www.mosaicmicro.com/>

Primary CNF Tools Used: ABM Mask Aligner, AJA Sputter System(s), Bruker DektakXT Profilometer, CHA Mark 50 E-beam Evaporator, Class 1 Photolithography Spinners, Class 2 Photolithography Spinners, GCA AS200 Stepper, Hamatech Wafer Processor(s), Heidelberg MLA 150 Maskless Aligner, Oxford 82 RIE, Oxford PECVD, PT 720-740 RIE, YES Asher

Abstract:

Glass substrates have excellent electrical and mechanical properties which have led to an increasing interest for their use in advanced microelectronic and photonic packaging applications. Glass substrates offer a very low loss tangent at GHz frequencies, while being moisture insensitive and dimensionally stable. This work outlines a novel approach for fabrication of interposers using thin glass (200 micron and below), normally difficult to handle in standard processes. The process yields void-free, hermetic, copper-filled precision through glass vias (TGVs), along with redistribution layer (RDL) fabrication with up to three metal redistribution layers per side. Furthermore, Mosaic Microsystems is developing various methods to integrate photonic waveguides with thin glass interposers to match high-speed electronics packaging with high-speed photonic communication.

Summary of Research:

Due to Mosaic's patented Viafirm® bonding technology it is possible to process 100 mm, 150 mm, and 200 mm thin glass wafers with the conventional silicon processing equipment at the CNF. RDL fabrication utilizes the photoresist spinners and the ABM Mask Aligner for contact alignment or the GCA AS200 Stepper for features that require near micron resolution. Electron-beam evaporation of various metal layers has been performed using the CHA Mark 50 E-beam Evaporator.

In addition, our team uses the Hamatech HMx900s auto wafer developers to develop double layer liftoff resist structures applied at CNF. Analysis tools at CNF such as the Filmetrics F50 and Keyence microscope aid in resist and final pattern analysis.

Conclusions and Future Steps:

We have successfully fabricated multi-layer RDL thin glass interposers. Our more recent work has focused on the fabrication of highly precise thin film resistors as well as microfluidic channels incorporated into the thin glass interposer. For the future, we will continue to improve upon our processes at CNF to deliver upon our customer's needs. We will also continue to develop methods of incorporating photonic waveguides with the thin glass interposers, of which key elements will occur at CNF.

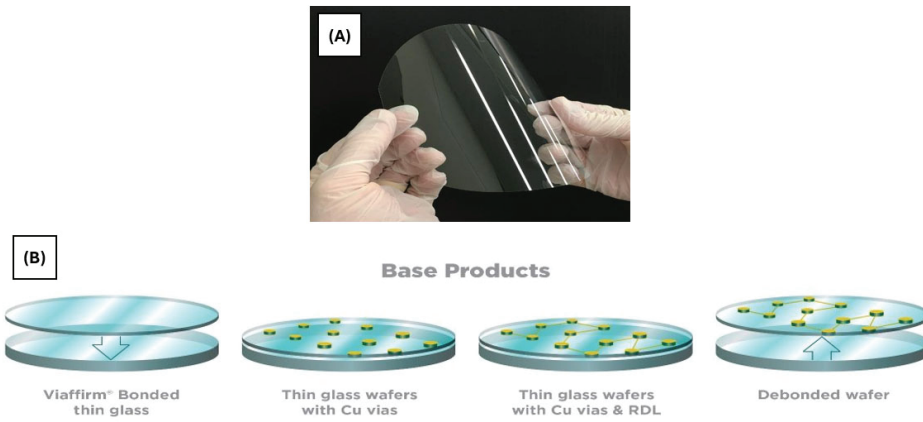


Figure 1: (A) Demonstration of the flexibility of thin glass. (B) Schematic outlining Mosaic's robust Viafirm® bonding process.

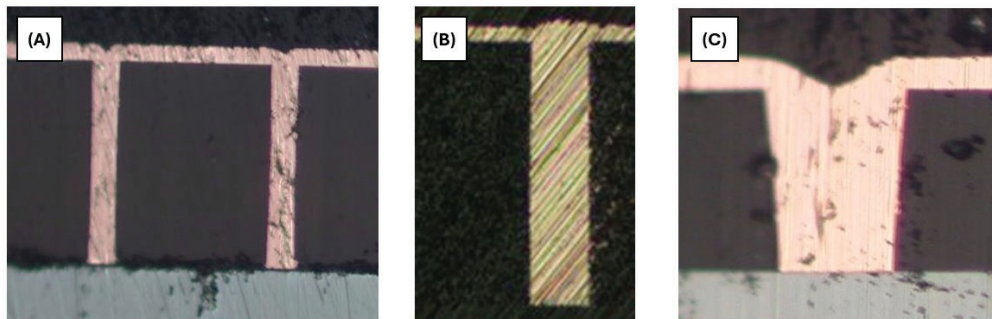


Figure 2: Cross-sections of fully filled copper vias with varying shapes and diameters. (A) 15 μm columnar via, (B) 25 μm columnar via, and (C) 35 μm tapered via.

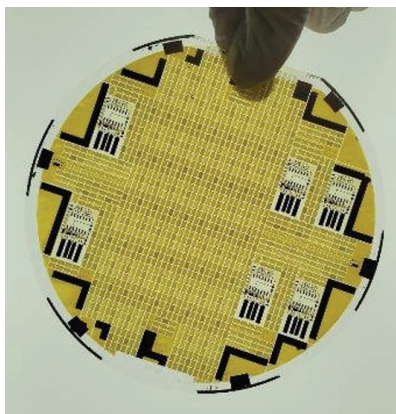


Figure 3: Example of a fully fabricated thin glass interposer with through glass vias and multiple redistribution layers.

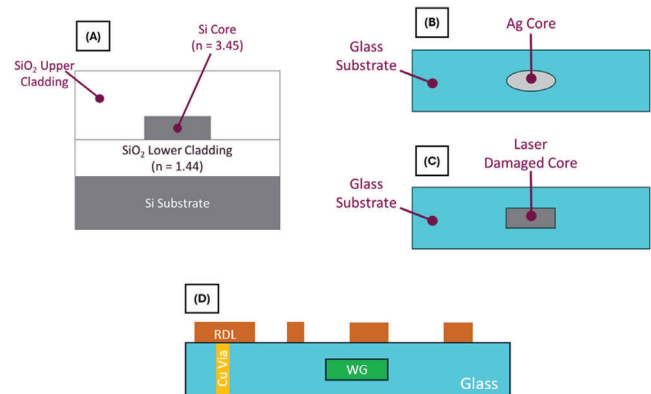


Figure 4: Schematic of various photonic waveguides. (A) Traditional silicon waveguide, (B) Ion-exchange waveguide, (C) Ultrafast laser inscription waveguide, and (D) Integration of electrical and optical communication.

electrical and optical communication.

Metal-Containing Resists for Extreme Ultra Violet

CNF Project Number: 3108-23

Principal Investigator(s): Robert L. Brainard

User(s): Munsaf Ali, Moira Niluxsshun, Harry Weinstein, Stephen Smith, Ryan Chae

Affiliation(s): Department of Nanoscale Science and Engineering, University at Albany, SUNY; Samsung-SDI

Primary Source(s) of Research Funding: Samsung-SDI

Primary Source(s) of Research Funding: U.S. Department of Defense (DOD), Customer Contracts

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Primary CNF Tools Used: JEOL E-beam 6300, Woollam RC2 Spectroscopic Ellipsometer, Zeiss Supra SEM, Zeiss Ultra SEM

Abstract:

Since 2011, our group has developed Extreme Ultra Violet photoresists composed of amorphous thin-films of compounds containing tin, cobalt, platinum, palladium, bismuth and antimony in our project called Molecular Organometallic Resists for EUV (MORE).¹⁻⁹ This project focuses on the development and characterization of metal-containing photoresist platforms for Extreme Ultra Violet lithography applications. Our goal is to develop materials suitable for both positive- and negative-tone EUV resists and E-beam resists. We leveraged Cornell Nanoscale Facility's nanofabrication and characterization capabilities to carry out E-beam lithography and SEM analysis of these platforms.

Summary of Research:

Platform Selection: Focus on Reproducibility

We prioritized work on organo-metallic resists, which showed promising initial results but suffered from reproducibility issues. Addressing this is foundational to ensuring consistent performance in both academic research and industrial integration.

CNF Usage and Progress

Between August 2024 and June 2025, we conducted multiple visits to CNF, steadily increasing the productivity of each session:

Imaging Trips Schedule

- CNF 3: Aug 12, 2024
- CNF 4: Oct 2, 2024
- CNF 5: Jan 13, 2025
- CNF 6: Apr 1, 2025
- CNF 7: Jun 25, 2025

Over time, our group; Increased participation (from 2 to 4 researchers per trip), conducted process planning

meetings beforehand, reduced screening of new platforms in favor of optimizing high-performing candidates, improved familiarity with lithography and SEM tools

A significant improvement came from reducing beam current from 10 nA to 1 nA, dramatically increasing pattern fidelity and visibility via SEM and optical microscopy.

Technical Achievements

- Developed contrast curve data across several resist formulations (Figure 2).
- Achieved high-resolution imaging of both positive- and negative-tone resists
- Increased resolution from 50 nm to 20 nm using the JEOL 6300
- Demonstrated excellent line edge roughness (LER) in optimized formulations
- Used RC2 ellipsometry to monitor film thickness pre- and post-development

Figure 3 and Figure 4 present representative SEMs of successful patterns, showing clear resolution improvement.

Conclusions and Future Steps:

Our CNF trips became increasingly effective as the team-built process familiarity and focused on materials with the most promise. Key future work includes:

- Continued reproducibility studies of organo-molecular resists
- Further dose optimization and LER analysis
- Testing of various development protocols on positive and negative tone resist platforms
- Continued e-beam lithography and SEM imaging of optimized resists

CNF-#	Start Date	Current (nA)	Total Wafers	Total Exposures	Number of Samples Exposed			Number of Visible Patterns	
					CC	Standard L/S	High Res L/S	OM	SEM
CNF-1	9/8/2023	1	2	2	-	2	-	1	1
CNF-2	11/13/2023	1	6	6	-	6	-	5	4
CNF-3	8/12/2024	1	31	61	26	35	-	24	11
CNF-4	10/2/2024	10	45	180	40	145	-	13	4
CNF-5	1/13/2025	1	48	192	40	144	8	108	75
CNF-6	4/1/2025	1	36	144	44	76	24	52	45

Figure 1: Shows lists experimental details from each visit.

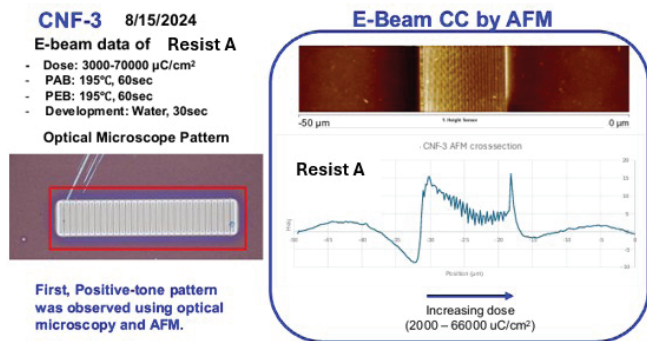


Figure 2: Positive-tone pattern Observed using optical microscope and AFM.

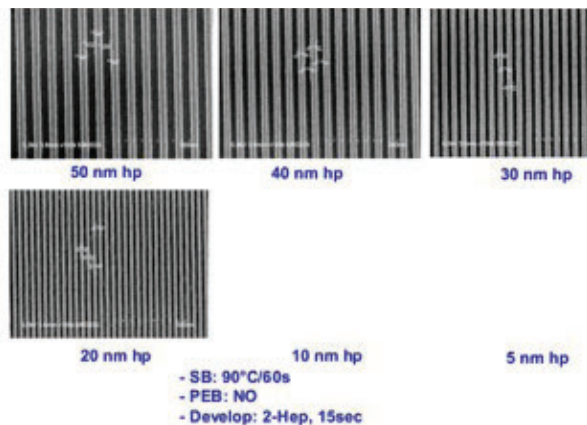


Figure 3: SEM image of negative tone resist B at 20 nm resolution (non-confidential)

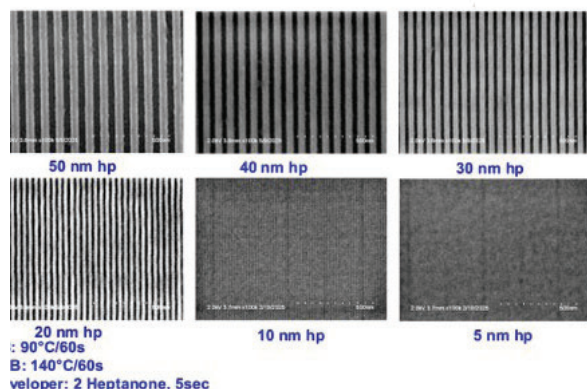


Figure 4: SEM image of negative tone resist B at 20 nm resolution (non-confidential)

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Electrospray Propulsion Time-of-Flight Secondary Ion Mass Spectrometry Diagnostic

CNF Project Number: 3242-25

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Primary CNF Tools Used: C4500 Odd-Hour Evaporator, Zygo Optical Profilometer, AJA Sputter

Abstract:

Electrospray thrusters are electric propulsion systems offering exceptional thrust-to-propellant weight efficiency in scalable form factors. However, system lifetimes are constrained by ion plume interception of downstream electrodes, where high-energy impacts (>1 keV) cause sputtering and secondary ion emission. These secondary ions indicate electrode degradation and electrochemical processes that limit system longevity. An electrospray propulsion secondary ion mass spectrometry diagnostic was developed to investigate ion plume-surface interactions across operational parameters. The system features a single, externally-wetted tungsten ion source with ionic liquid propellants, electron beam-evaporated metallic targets, and linear time-of-flight mass spectrometry. Silver target impacts demonstrate clear target sputtering through detection of silver and silver cluster ions, alongside propellant-related secondary ion markers, enabling comprehensive characterization of lifetime-limiting mechanisms.

Summary of Research:

Electric space propulsion systems generate thrust by accelerating propellant through electric and magnetic fields, offering superior fuel efficiency compared to chemical propulsion since exhaust velocity depends on applied power rather than chemical bond energy constraints [1].

Electrospray micropropulsion thrusters utilize electrostatic fields to extract and accelerate charged particles from liquid propellant at sharp emitter tips [2,3]. When kilovolt-level potentials are applied between the emitter and downstream extractor electrode, surface tension, electric, and hydrodynamic stresses form a Taylor cone. This induces ion emission through field emission evaporation, accelerating ions to velocities exceeding 10,000 m/s and generating thrust ranging from nanonewtons to micronewtons per emitter [4,5].

Many electrospray devices employ chemically complex room temperature ionic liquids (RTILs) as propellants, comprising organic cations and anions

such as 1-ethyl-3-methylimidazolium tetrafluoroborate (EMI-BF₄) and 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMI-Im) [6,7]. These propellants are attractive for their nonvolatile properties and bipolar operation capability, eliminating

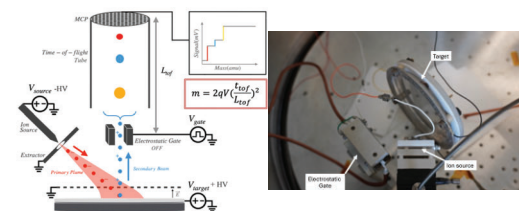


Figure 1 (left): Schematic of the electrospray propulsion TOF-SIMS diagnostic, where the ion source directs the ionic liquid primary beam at the target, where secondary ion emission is induced and directed toward the electrostatic gate and time-of-flight system with an MCP detector. The polarities of the two ion beams are reversed to collect negative secondary ions.

Figure 2 (right): The diagnostic as installed in the vacuum testing facility, including the ion source, the target created via e-beam evaporation, and the electrostatic gate portion of the linear time-of-flight spectrometer.

external neutralizer requirements. This combination makes RTIL electrospray thrusters ideal for missions requiring efficient, compact, low-mass, and low-power propulsion systems [8].

High-energy electrospray plume impacts (>1 keV) induce target surface sputtering, producing secondary ions that interact with electrostatic fields during thruster operation and testing [11]. Understanding their chemical composition is crucial for system performance characterization [12].

A novel electrospray time-of-flight secondary ion mass spectrometry (ESI TOF-SIMS) diagnostic was developed to characterize plume-surface interactions, as shown in Figure 1 and Figure 2. The experimental design features: (a) a tungsten single emitter primary electrospray ion source externally wetted with ionic liquid, (b) a high-voltage target assembly with secondary ion acceleration grid, (c) an electrostatic deflection gate, (d) a time-of-flight tube, and (e) a microchannel plate detector [13].

The primary molecular ion plume impacts a target surface

at controlled incidence angles with energies dependent on source and target potentials. High-energy impacts remove secondary electrons, atoms, molecules, and ions from the target surface. Secondary ions of selected polarity are extracted via potential differences between the high-voltage target and grounded acceleration grid, creating a single-polarity, approximately monoenergetic beam that passes through the pulsed electrostatic deflection gate and down the linear time-of-flight tube to the detector.

The target consists of a 100 mm diameter silicon wafer with 100 nm silver deposition via e-beam evaporation using the CNF CVC4500 evaporator. Silver was selected for its two readily identifiable isotopes (^{107}Ag and ^{109}Ag) with nearly equal natural abundances, providing ideal detection and calibration capabilities. Atomically flat, uniform metallic surfaces ensure consistent SIMS signals, as surface topology variations can compromise analysis reliability.

Initial positive secondary ion analysis from a negative electrospray plume impacting a silver target is shown in Figure 3. This spectrum resolves numerous species below 100 amu, notably the hydrogen cation, boron isotopes, and numerous spectral 'families' depicting hydrocarbon-related peaks related to the organic primary impacting ions and/or oil contamination. In addition, peaks at 107, 109, 216 and 324 amu indicate sputtering of the target through detection of silver isotopes and silver cluster ions. Negative secondary ion spectra show the presence of fluorine ion in addition to cyanide and hydrocarbon ions. Initial results show multiple, distinct secondary species that not only prove the capability of the diagnostic but reveal secondary ions that limit the lifetime of electrospray systems [13,14].

Recent work has focused on analyzing secondary ions that form with propellant thin films as the target. The motivation for such work is due to the fact that over time, propellant accumulates on downstream electrodes in electrospray thruster systems. Therefore, at a certain point the secondary ions formed from propellant overspray is independent of the electrode material and entirely dependent on the accumulated propellant. This work has involved producing silver targets utilizing the CNF CVC4500 evaporator, spin coating these wafers with solvent/ionic liquid mixtures and bombarding the thin-film target in the ESI TOF-SIMS diagnostic and analyzing the secondary ions formed. Species from the baseline tests remain present (H^+ , B^+ , C_nH_m^+), with additional features that mark the presence of the ionic liquid including the imidazole ring at 83 amu and the imidazole ring with the methyl chain at 96 amu, and most notably the full primary ion cation detection at 111 amu.

Post processing of the thin-film silver target by the Zygo optical profilometer at CNF, as shown in Figure 4, shows sputtering on the order of 100s of nm over the course of ~6 hour beam exposure to the target. The grid-like pattern is a product of the diagnostic mechanical setup, as the primary beam passes through a grounded transparent stainless-steel mesh that maintains the necessary electric fields before impacting the target.

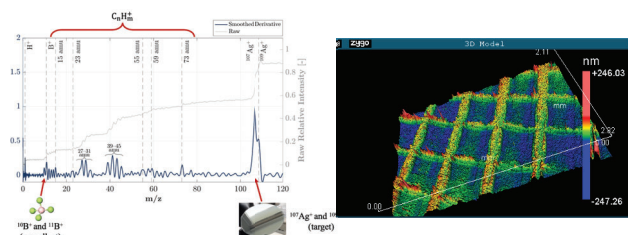


Figure 3 (left): Positive secondary ion mass spectrum from a 4 keV negative EMI-BF₄ plume impact with an Ag target, out to 120 amu. The dominant peaks were the silver ion isotopes, with clear signs of the propellant through detection of boron isotopes. Figure 4 (right): A 3D profile of the target after ion-plume bombardment over the course of 3 hours, showing the sputter depth due to beam exposure.

This information will be crucial in determining sputter rates moving forward.

Conclusions and Future Steps:

A novel electrospray time-of-flight secondary ion mass spectrometry diagnostic successfully characterized plume-surface interactions in electrospray thrusters. Using a tungsten ion source with ionic liquid propellant under vacuum conditions, clear secondary ion emission in both polarities is confirmed, establishing the viability of electrospray TOF-SIMS for thruster analysis. Future work will determine secondary ion origins to distinguish target contamination from primary plume fragmentation, critical for separating intrinsic thruster effects from facility artifacts. Characterizing like-polarity secondary ions requires diagnostic modifications including acceleration stages and target biasing to overcome signal degradation below 2 keV. These enhancements will enable comprehensive analysis across varying operating conditions, propellants, and surfaces, providing insights into plume-surface interactions affecting spacecraft contamination and thruster performance.

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