Reliable Scanning Tunneling Microscopy Prepared Fabrication for 2D Quantum Material Device Research

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Primary CNF Tools Used: Heidelberg DWL 2000 Mask Writer, GCA AS200 i-line Stepper, Oxford Plasmalab 81/82 RIE, SC4500 Odd-Hour Evaporator, DISCO Dicing Saw

Abstract:

This report introduces a novel fabrication methodology enabling the reliable production of scanning tunneling microscopy (STM) prepatterned chips for micro-level 2D material flake identification. By integrating precision photomask design, optimized interfacial metal stacks, and defect-minimized processing, we achieved >95% yield in devices capable of targeting sub-5μm flakes. The process establishes a new baseline for reproducible quantum material research platforms.

Summary of Research:

STM achieves atomic resolution but suffers from an intrinsically small field of view (~1 μm), rendering navigation to specific micron-scale samples (e.g., 2D flakes) slow and prone to tip crashes. External localization aids are impractical in extreme environments [1, 2]. In CNF, we developed recipes for prepatterned chips with integrated registration markers to resolve this by enabling reliable STM navigation to target flakes without external systems.

1. Precision Photomask Engineering

Critical to pattern making was developing quartz 5-inch photomasks with alignment markers resolvable at 199 nm scales. Using the Heidelberg DWL 2000, AutoCAD-designed patterns underwent .dxf to .gds conversion in KLayout with manual correction of alphanumeric fiducials (design pattern see Fig. 1). This eliminated coordinate driŌ during stepper alignment, enabling consistent placement of μm level registration markers essential for 2D quantum device targeting. Post-write verification included Hamatech Process 2 cleaning and 60s Cr etching (Process 1) to ensure defect-free surfaces.

2. Lithography for Flake-Scale Features

A bilayer resist system (LOR3A/SPR700) was optimized for STM-specific undercut profiles, comprising an adhesion layer of P20 at 3000 rpm (15s), undercut control via LOR3A (4000 rpm, 180°C/5min bake), and an imaging layer of SPR700 (3000 rpm, 90°C/1min bake). GCA iline exposure at focus = -6, dose = 0.22 produced 800 nm apertures with tapered sidewalls (70° angle), verified by cross-section SEM. Post-development O_2 descum (Oxford RIE, 60W, 25s) prevented resist scumming around critical edges.

3. Interfacial Engineering for Flake Contact

Two metallization strategies enabled reliable flake-electrode interfaces: edge contacts with 3.5nm Cr / 15nm Pd evaporated at 0.5Å/s (1×10^{-6} Torr), and scanning pads with 50nm Cr at 4Å/s (4×10^{-6} Torr). The Cr/Pd bilayer provided oxidation-resistant surfaces while maintaining atomic-scale flatness, critical for STM tip stability during flake characterization.

4. Damage-Mitigated Device Release

LiŌoff utilized inverted 1165 solvent immersion (3hr) to preserve delicate flake-search electrodes, followed by dicing protection via PMMA 495 A4 coatings (2000 rpm, 170°C bake) to reduce edge fractures, with back-polishing to manually remove the insulating SiO_2 layer. Cutting was conducted under a DISCO Dicing saw along predefined lines, and final plasma cleaning employed sequential 200W O_2 strips (Oxford RIE) to remove organics without ion bombardment damage.

Final chips showed >90% electrode integrity (Fig. 2) and have been used for more than 100 STM 2D quantum device making. Reliability validation involved ~200 STM_v2 chips processed across two wafer lots, demonstrating functionality in locating 2-10μm flakes (Fig. 3), zero registration failures during 2D material transfers, and half a year shelf-life stability (N_2 storage).

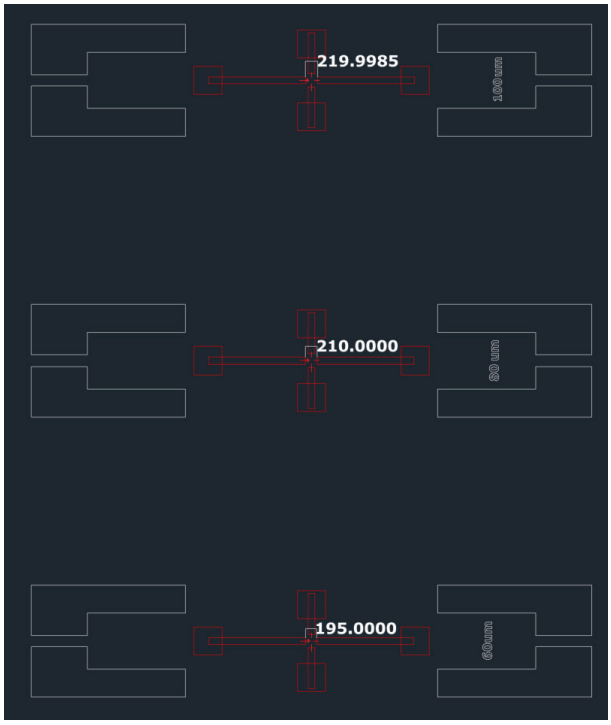

Fig. 1: STM_v2 mask design showing 3μm alignment markers.

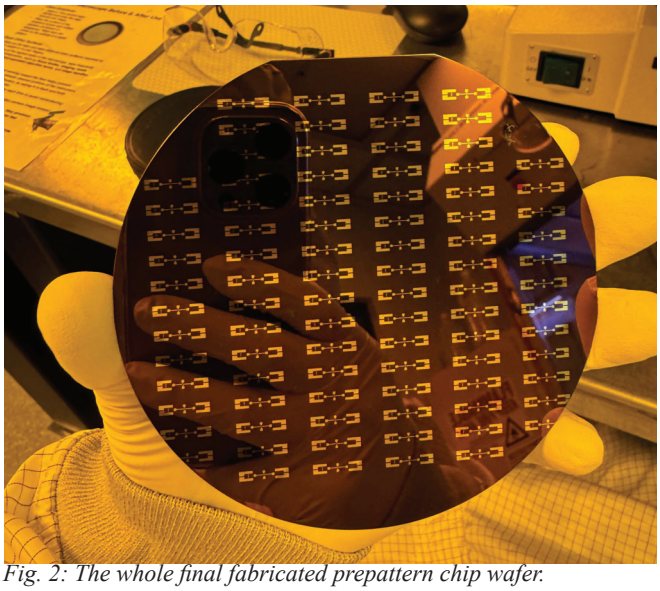

Fig. 2: The whole final fabricated prepattern chip wafer.

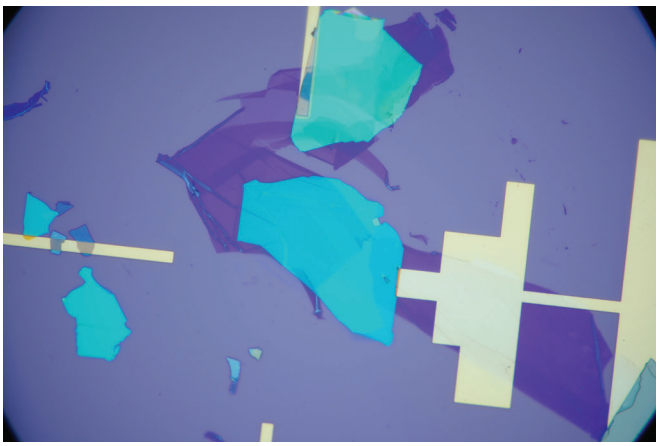

Fig. 3: Optical micrograph of a graphene-based 2D device on an STM prepattern chip.

Conclusions and Future Steps:

The established process enables reliable fabrication of STM prepatterned chips for microscale 2D flake discovery, achieving >95% yield in registration-critical devices. Future work will extend this methodology to air-sensitive materials (e.g., $CrPS_4$) via glovebox-compatible integration, requiring conductance-optimized electrodes through testing new electrode categories to minimize conductance reduction and geometric redesign through modifying pad geometries to prevent bonding-induced circuit shorts.

References:

[1] Li, G., Luican, A., & Andrei, E. Y. Rev. Sci. Instrum. 82, 073701 (2011)

[2] Liu, X., et al., Science 375, 321-326 (2022)