

Gate-tunable electroresistance in a sliding ferroelectric tunnel junction

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Abstract:

Ferroelectric tunnel junctions are an attractive platform next-generation memory applications due to their capacity for non-volatile operation and non-destructive readout of the electrical polarization. Generating a tunneling current that is sensitive to the polarization state requires a tunneling potential profile that is mirror asymmetric. This asymmetry has been engineered in previous work by using electrode layers with mismatched densities of states [1] or dielectric spacer layers directly within the tunnel barrier [2]. Here, we show that by fabricating ferroelectric tunnel junctions with an electrostatic gate, the tunneling conductance can be sensitive to the polarization state even when the two electrode layers are both monolayer graphene and there is no dielectric spacer layer. The magnitude and sign of the resulting tunneling electroresistance can be controlled by the bias and gate voltage of the junction.

Summary of Research:

In a ferroelectric tunnel junction (FTJ), two conducting layers sandwich an insulating ferroelectric tunnel barrier. Achieving appreciable readout currents with conventional ferroelectrics is challenging since depolarization fields, which increase with decreasing film thickness, can destabilize ferroelectric order in ultra-thin layers. Van der Waals ferroelectric materials, however, can sustain ferroelectric polarizations with no critical thickness limit. Recently discovered van der Waals sliding ferroelectrics offer a novel mechanism for ferroelectric switching that also promises higher endurance compared to non-sliding ferroelectrics [3-5].

In our devices, we mechanically assemble parallel bilayer boron nitride (P-BBN) with graphene electrodes on either side. The heterostructure is encapsulated by hexagonal boron nitride dielectric layers with a bottom graphitic gate. Figure 1 shows a schematic of the device geometry. To make electrical contact to the graphene

electrode and graphite gate layers, we perform electron beam lithography (Zeiss Supra SEM and Nabity Nanometer Pattern Generator System) and reactive ion etching (Oxford 81 Etcher) to first expose edges of the conducting layers. We then deposit Ti/Au contacts with electron beam deposition (Angstrom Evaporator). Figure 2 shows a micrograph of a completed device.

Transport measurements are performed at $T = 4.2\text{K}$. We measure the differential conductance dI/dV of the junction by applying a small AC bias (1 mV) as we sweep the DC bias, V , and read out the resulting AC current. The gate voltage, V_G , is fixed during each bias sweep. The left panel of Figure 3 shows the tunneling conductance on a forward and backward sweep of the DC bias. The tunneling conductance is nonlinear and increases with bias voltage, indicating that the P-BBN acts as a good insulating barrier. Step-like features in the conductance are likely due to inelastic electron tunneling assisted by phonons in the barrier or electrode layers. The tunneling conductance is hysteretic with the bias and can be quantified by the tunneling electroresistance

$$\text{TER} = 100 \times \frac{G_f - G_b}{G_f + G_b} \quad \text{where } G_{f(b)} \text{ is the conductance of}$$

the forward (backward) bias sweep.

Notably, the magnitude and sign of the TER vary strongly with DC bias. At $V_G = -1.0\text{ V}$, Figure 3 right panel, a positive peak appears at negative bias while a negative peak is present at positive bias. By varying the gate, the bias dependence of the TER can be controlled. Figure 4 shows the same data as Figure 3 but now taken at $V_G = 5.4\text{ V}$. Now, a negative (positive) peak is present at negative (positive) bias, which is opposite the signal at $V_G = -1\text{ V}$ (Figure 3 right panel).

In summary, we have shown that the conductance graphene/P-BBN/graphene tunnel junction is sensitive

to the polarization state of ferroelectric P-BBN. The magnitude and sign of the resulting TER can be tuned by the bias and gate voltage.

References:

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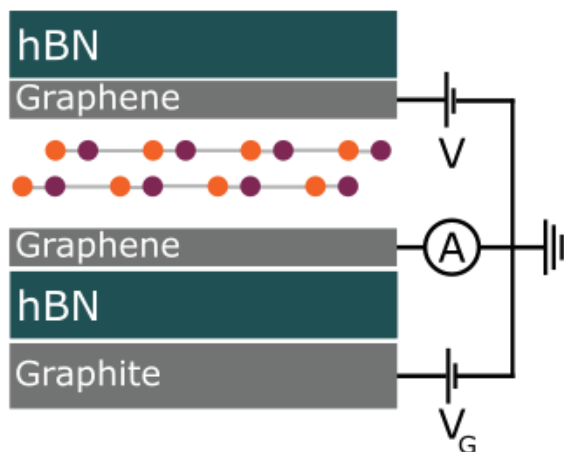


Figure 1: Device schematic of graphene/P-BBN/graphene tunnel junction. A bottom graphite gate is used to tune the carrier densities of the two graphene layers.

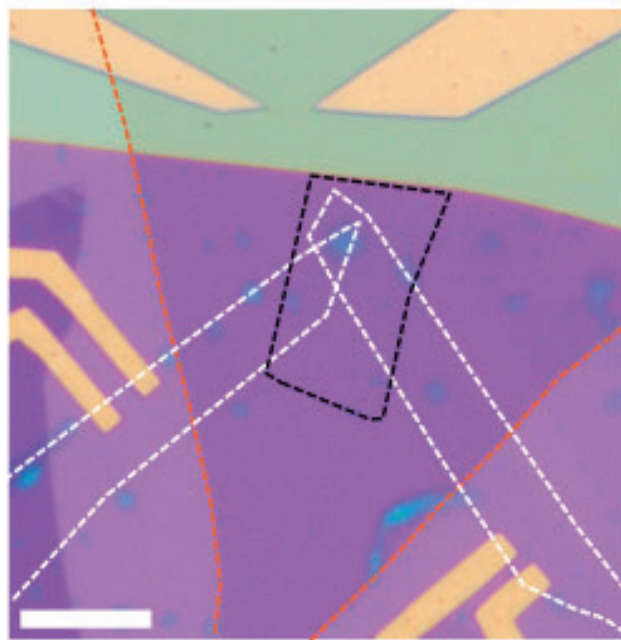


Figure 4: Same as Figure 3 but at $V_G = -5.4$ V.

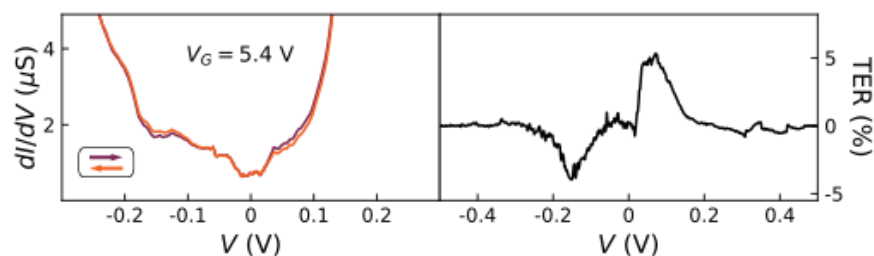


Figure 2: Micrograph of device. The graphene electrodes, P-BBN, and graphite gate electrode are outlined in dashed white, black, and orange lines, respectively. The scale bar is 10 μm

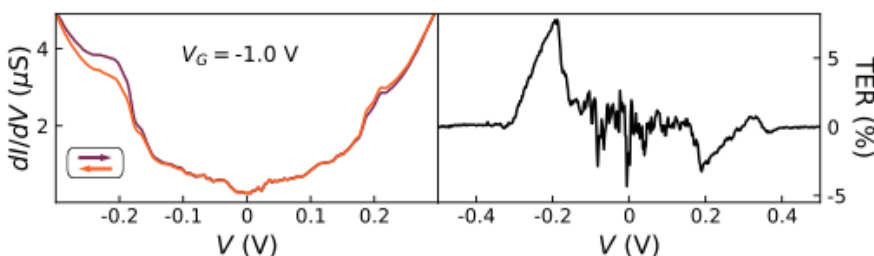


Figure 3: Left: Tunneling conductance as a function of bias voltage at constant gate voltage $V_G = -1.0$ V. The forward (backward) sweep is shown in purple (orange). Right: TER calculated from the data on the left panel.