Reducing the Operating Voltage of Deep-Ultraviolet Light Emitting Diodes

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Principal Investigator(s): Debdeep Jena and Huili (Grace) Xing
User(s): Sheena (Hsin Wei) Huang

Affiliation(s): Electrical and Computer Engineering, Cornell University

Primary Source(s) of Research Funding: DARPA

Contact: djena@cornell.edu, hh494@cornell.edu

Research Group Website: https://jena-xing.engineering.cornell.edu/

Primary CNF Tools Used: PT770 ICP-RIE, Oxford PE-ALD, E-beam evaporator, AS 200 I-line stepper, Heidelberg MLA, Ultra SEM, PE-CVD, Woollam RC2 ellipsometer

Abstract:

Improving the electrical efficiency of deep-ultraviolet light emitting diodes (DUV- LEDs) based on the ultrawide bandgap material AlGaN is important for applications in disinfection, sensing, and lithography. Reducing the contact resistance of the device is crucial to improving the electrical efficiency. For high-performance electronic and optoelectronic devices, specific contact resistivities (ρ_c) on the order of 10^{-5}-10^{-6} Ωcm^2 are typically required. However, the ultrawide bandgap nature of AlGaN alloys poses intrinsic difficulties in achieving such low-resistance contacts. In this study, we investigate the co- optimization of p-InGaN and n-AlGaN contacts of DUV LEDs in monolithic integration.

These diodes are grown pseudomorphically on bulk AlN substrates by molecular beam epitaxy (MBE), resulting in low threading dislocation density and allowing for internal quantum efficiency (IQE), carrier injection efficiency (CIE), and lifetime of devices. The goal of this work is towards an electrically-injected DUV laser diode grown by MBE.

Summary of Research:

We find that using a thin $In_{0.07}Ga_{0.93}N$ cap is effective in achieving ohmic p-contacts with specific contact resistivity of 3.10×10^{-5} Ωcm^2. Upon monolithic integration of p- and n-contacts for DUV LEDs, we find that the high temperature annealing of 800 °C required for the formation of low resistance contacts to n-AlGaN severely degrades the p-InGaN layer, thereby reducing the hole concentration and increasing the specific contact resistivity to 9.72×10^{-4} Ωcm^2. Depositing a SiO_2 cap by plasma-enhanced atomic layer deposition (PE-ALD) prior to high temperature n-contact annealing restores the low p-contact resistivity, enabling simultaneous low-resistance p- and n-contacts.

DUV-LEDs emitting at 268 nm fabricated with the SiO_2 technique exhibit a 3.5 V reduction in operating voltage at a current level of 400 A/cm^2 and 1.9 mΩcm^2 decrease in differential ON-resistance. This study highlights a

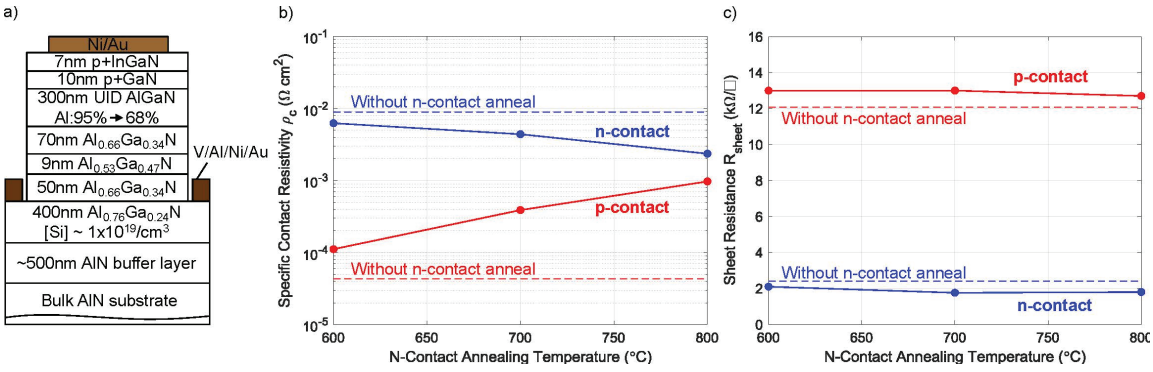

Figure1: (a) Heterostructure of the DUV LED samples used for this contact annealing temperature-dependent study. (b) Specific contact resistivity of n- and p-contact vs n- contact annealing temperature. P-contacts were subsequently annealed at 450 °C. All resistance values were extracted at 1 mA from CTLM-IV measurement. (c) Sheet resistance vs n-contact annealing temperature.

scalable route to high-performance, high-Al-content bipolar AlGaN devices.

Conclusions and Future Steps:

We are continuing to reduce the contact resistance of the p- and n-contacts through different metallization annealing conditions, metal stack, and acid treatment. We would also like to experiment with different capping materials like SiN and AlN to further reduce the degradation of p-InGaN during n-contact anneal.

References:

[1] Appl. Phys. Express 12, 124003 (2019)

[2] Advanced Electronic Materials 11, 2300840 (2025)

[3] Applied Physics Letters 124, 102109 (2024)

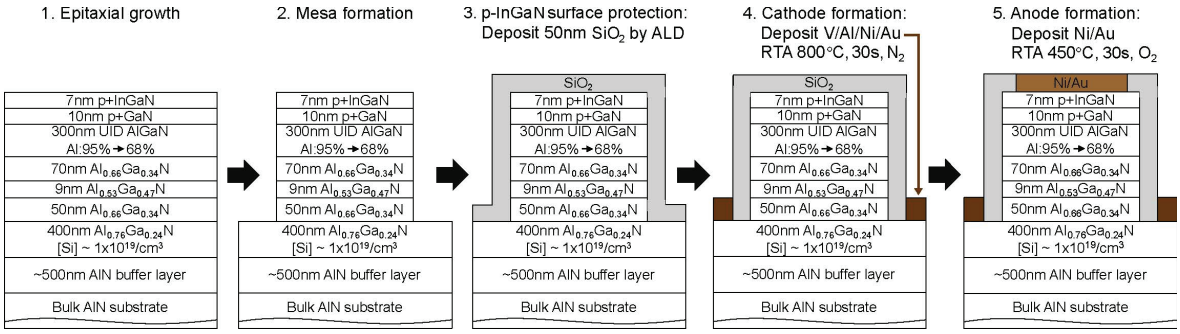

Figure 2: Schematic diagram illustrating the fabrication process of an LED with the SiO2 capping technique.

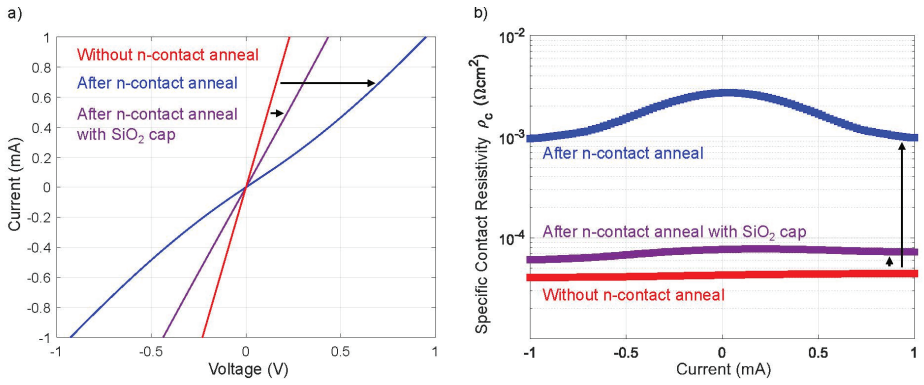

Figure 3: (a) CTLM-IV curves comparison of p-contact without undergoing n contact anneal, after undergoing n-contact anneal with SiO2 cap, and after undergoing n-contact anneal without SiO2 cap. IVs are plotted for 2 μm spacing. (b) Resistance vs metal electrode spacings for the data shown in (a).

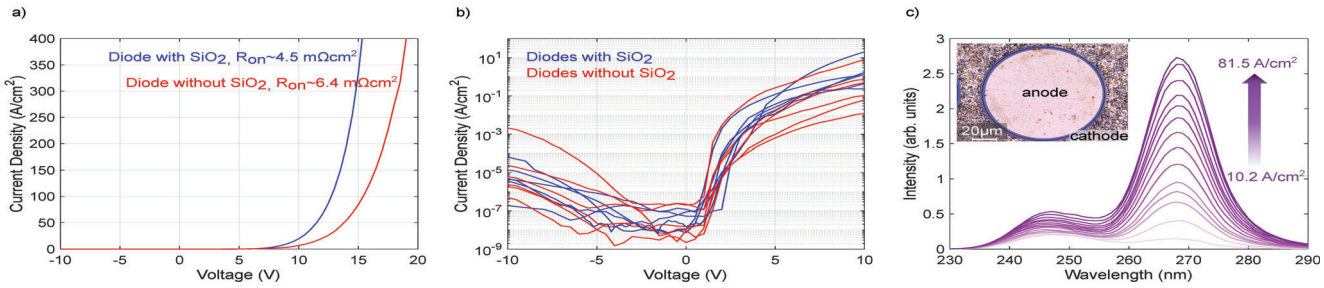

Figure 4: (a) Room temperature J-V characteristics of two LEDs, one with SiO2 capping method and one without. The diferential ON- resistance was extracted at 400A/cm2. (b) IV from batch test of LEDs with and without SiO2 capping. (c) Room temperature electroluminescence of an LED with the SiO2 capping method. Inset shows the microscopy image of a fabricated LED.