Isotropic Plasma ALE of Nitride Semiconductors

CNF Project Number: 280019
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Primary CNF Tools Used: Takachi ALE

Abstract:

This study demonstrates the successful atomic layer etching of aluminum nitride and gallium nitride using sequential exposures to SF_6 plasma for surface fluorination, followed by Cl_2/BCl_3 plasma to remove the altered layer at 100 °C. We investigated the etch rates, the self-limiting behavior of the reactions, and their combined effect, aiming to better understand the underlying etching mechanism. A range of analytical tools was employed, including in-situ spectroscopic ellipsometry, X-ray photoelectron spectroscopy (XPS), and atomic force microscopy (AFM).

Summary of Research:

Gallium nitride (GaN) and aluminum nitride (AlN), both belonging to the III–V semiconductor group, play a pivotal role in modern electronic and photonic technologies. Their wide bandgaps, strong thermal stability, and intrinsic piezoelectric properties make them particularly suitable for fabricating high electron mobility transistors (HEMTs), which are commonly used in radio-frequency (RF) and power electronics applications[1–3]. Additionally, due to their outstanding optical characteristics, GaN and AlN are also emerging as key materials for photonic integrated circuits and light-emitting diodes (LEDs)[4,5].

As device architectures continue to evolve in complexity and scale, there is a growing demand for more sophisticated processing techniques. One such advancement is the development of enhancement-mode (E-mode) HEMTs, which are especially desirable for applications such as power conversion and industrial power systems[6,7]. The fabrication of efficient and robust E-mode HEMTs often requires the formation of recess gate structures[8,9]. However, traditional dry etching methods have notable limitations, often inducing damage to the surface and the two-dimensional electron gas (2DEG), which negatively impacts device performance[10]. To address these challenges in next-generation devices, atomic layer etching (ALE) has emerged as a promising alternative to conventional etching techniques[11,12].

ALE operates on the principle of dividing the etching process into a series of self-limiting, sequential steps. This separation allows for precise control over the formation and transport of reactive species, enabling improved process uniformity and avoiding the surface damage typically associated with reactive ion etching. The ALE cycle generally comprises two distinct phases: a surface modification step that lowers the material's surface binding energy, followed by a removal step[13,14].

Utilizing SF6 plasma for surface modification and Cl_2/BCl_3 plasma for removal, we achieved etch rates of 4.4 Å/cycle and 5.7 Å/cycle for AlN and GaN respectively, which correspond approximately to one unit cell per cycle. Etch rates were monitored with in situ ellipsometry as seen in Figure 1. This approach displayed very controlled results, as well as self-limiting behavior when the duration of the removal step was changed, demonstrated in Figure 2. In order to prove that the ALE recipe obeys the fluorination and ligand exchange mechanism similar to thermal ALE, XPS spectra were utilized at different points of the cycle. During surface modification, a significant Al-F peak emerges, indicating the formation of AlF3. During removal, the peak reduces in intensity, indicating the formation of volatile AlCl3. The spectra are displayed in Figure 3. This ALE approach also achieves surface planarization, leading to a 21% roughness reduction as seen in Figure 4 for AlN.

References:

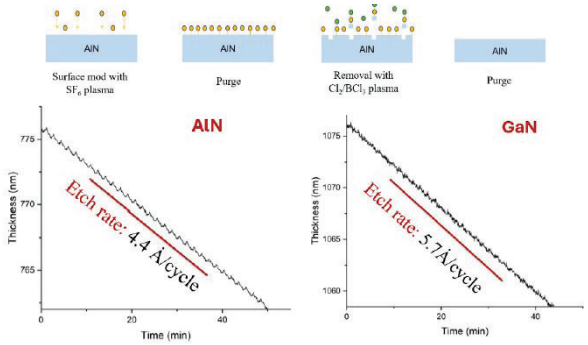

Figure 1: ALE cycle and etch rates for AlN and GaN

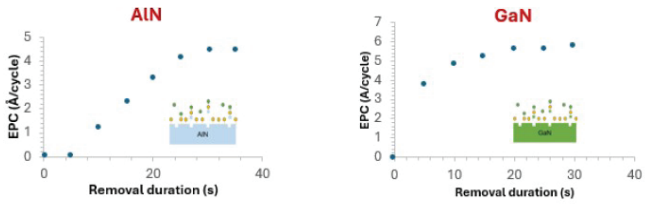

Figure 2: Removal step saturation curves for AlN and GaN displaying self-limiting behavior

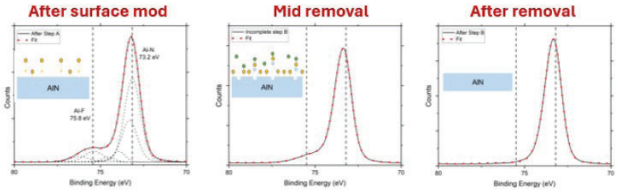

Figure 3: XPS spectra demonstrating fluorination and ligand exchange mechanism

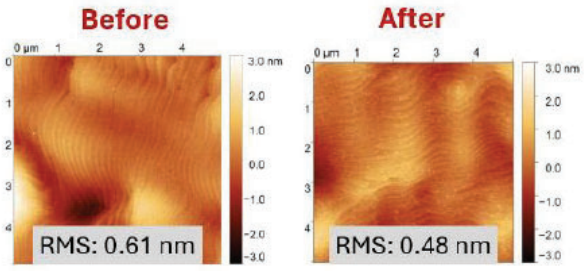

Figure 4: Surface morphology before and after etching for AlN

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High Frequency Micro-Patterned Fe65Co35 Thin Film with Tunable FMR and Permeability for RF Passives

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Primary CNF Tools Used: Microwave Small-Signal Probe Station and Electronics, Heidelberg MLA 150 Maskless Aligner, Keyence VHX-7100 Digital Microscope, SC4500 Odd-Hour Evaporator, AJA Sputter 3

Abstract:

This work presents a unique design method and optimization of high frequency magnetic patterns with controllable effective permeability and ferromagnetic resonance behavior for integrated microwave devices. Thin-film micro-patterned FeCo array with initial permeability of 42.7 has been fabricated to achieve a high FMR of 18.1 GHz. Independent control of magnetic properties of the pattern array has been realized by changing pattern spacing, showing a FMR tuning range of 2.20 GHz, with little change in effective permeability. Noise suppression and inductance enhancement at high frequencies (> 10 GHz) have been demonstrated for RF applications by integrating the proposed magnetic pattern array with coplanar waveguides (CPW). Our method shows a high degree of freedom and flexibility for designing high frequency integrated magnetic microwave components.

Summary of Research:

Fast growing demand of higher data rate, low latency, high quality of service in wireless communication systems calls for RF front-end devices that are frequency agile, miniaturized and multifunctional. Novel materials, structures and technologies have been explored to improve performance and bring new functionality for RF devices. Integrating high-performance novel magnetic materials into on-chip RF devices shows promising results in enhancing inductance, miniaturizing devices, suppressing interference and achieving non-reciprocity and tunability. Previous works have demonstrated the application of integrated magnetic materials in inductors, isolators, antennas, filters, and noise suppressors.

However, integrating magnetic materials for high frequency applications is particularly challenging. Limited by the relatively low ferromagnetic resonance (FMR) frequency, radio-frequency (RF) devices (e.g., on-chip inductors) integrated with common ferromagnetic materials consistently operate only at sub-GHz or up to a few GHz. While the FMR frequency can be increased by applying bias magnetic fields, this approach reduces the permeability of magnetic materials due to an intrinsic FMR-permeability tradeoff, therefore limiting the device performance. In addition, integrating large, localized bias magnetic fields with monolithic microwave circuits is highly impractical. Finally, the high loss of most ferromagnetic materials, especially near FMR frequency presents additional challenges for their device integration. Thus, novel magnetic materials with controllable high frequency characteristics are highly desired in microwave applications.

Previous work has shown promising results of improving FMR to a few GHz by patterning ferromagnetic thin films, yet no control of magnetic properties or design optimization of the magnetic pattern array has been proposed. In this work, we dramatically increase the FMR frequency of ferromagnetic patterns at zero field bias to 18.1 GHz, while maintaining a high broadband permeability of 42.7. An analytical model has been established to independently control and optimize the magnetic properties (ω_{FMR} and μ_r) of the patterned array by changing pattern spacing along two orthogonal axes. The proposed magnetic pattern array was integrated with CPWs to demonstrate its high frequency RF application for noise suppression and inductance enhancement. Our optimization approach allows for the facile design of integrated microwave magnetic components.

Conclusions and Future Steps:

In this work, we demonstrate design, tuning and optimization of patterned ferromagnetic thin film arrays for high frequency MMIC applications. The

FMR frequency of high permeability ferromagnetic patterns was increased to around 18 GHz (Ku band) for the first time. An analytical model was established, and a design method is proposed to independently tune the FMR, effective permeability of the magnet pattern array for optimal integrated device operation. The proposed pattern arrays were integrated with CPWs to experimentally demonstrate their RF applications as noise suppressors and inductors. Our method is highly versatile and provides a high degree of freedom for designing high frequency tunable magnetic properties for integrated microwave systems. In the future, we will implement a magnetic fully integrated inductor that works that high frequencies, and achieve tunability via magnetoelectric coupling.

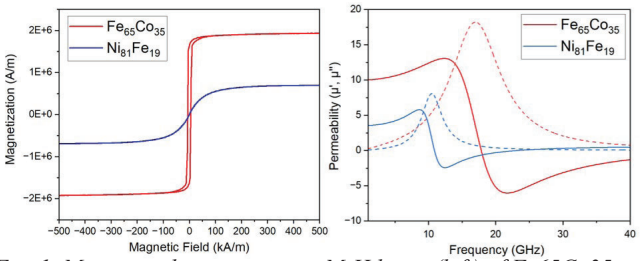

Fig. 1. Magnetic characterization M-H loops (left) of Fe65Co35 compared with Ni81Fe19 and frequency dependent permeability (right) calculated from the Landau-Lifshitz-Gilbert (LLG) model. The solid line and dash line represent the real part and imaginary part, respectively.

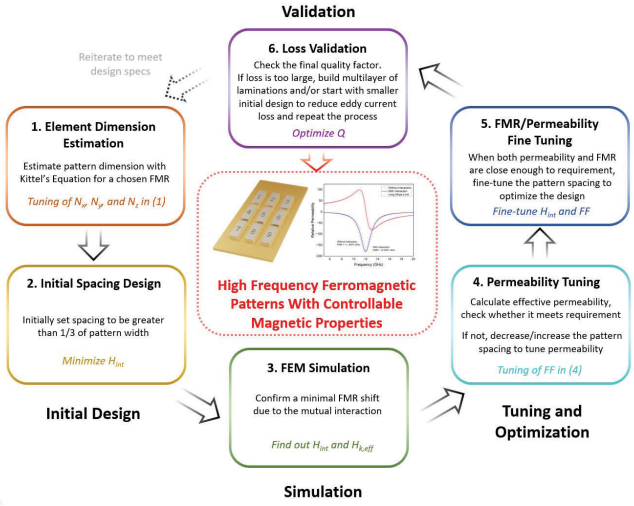

Fig. 2. Design flowchart for high frequency ferromagnetic patterns with controllable magnetic properties.

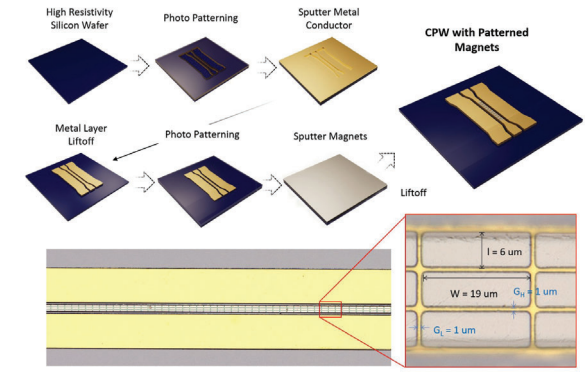

Fig. 3. Fabrication process and microscopic image of the Fe65Co35 magnet patterned CPW.

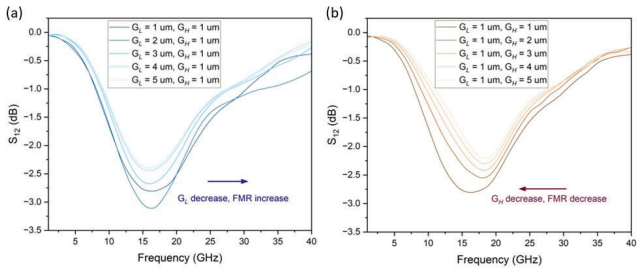

Fig. 4. Measured S12 parameters of noise suppressors when changing gaps of magnets along the (a) longitudinal (b) horizontal direction.

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Supramolecular Control of Ionic Retention in Hybrid Bilayer Synaptic Transistors

CNF Project Number: 306423
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Primary CNF Tools Used: ABM Contact Aligner, SC4500 Odd/Even-Hour Evaporator

Abstract:

The rise of big data and AI has exposed von Neumann architecture's limitations, spurring interest in computing paradigms that merge memory and processing. Artificial synapses, especially those based on electrolyte-gated transistors (EGTs) with ion-trapping layers, offer low voltage operation, robustness, and tunable retention. However, the molecular basis of ionic retention in these devices remains poorly understood.

Summary of Research:

Here, we report a supramolecular strategy to elucidate the molecular origin of ion retention in electrolyte-gated synaptic transistors. We designed a bilayer device comprising monolayer molybdenum disulfide (MoS_2) as the semiconducting channel and a polymeric ion-trapping layer incorporating dibenzo-18-crown-6 (DC), a cyclic host molecule known for its strong and size-selective binding to alkali metal ions (Fig. 1).1-2 Although crown ethers and their derivatives have been widely studied in ion recognition and transport, their potential to modulate ion retention dynamics in EGTs has been rarely explored.3-7 We fabricated the bilayer device using the following steps: To fabricate pre-patterned substrates, a 2-stage photolithography/e-beam deposition step was carried out on a 1 inch x 1 inch Si/SiO_2 piece to deposit source/drain electrodes and an SiO_2 insulating layer. Following this, we sequentially transfer a monolayer MoS_2 layer and DC-based thin film, thus yielding the final bilayer EGT device.

We show that ion retention in the DC layer is governed kinetically by ion concentration (Fig. 3) and thermodynamically by the competition between ion–host binding and ion solvation (Fig. 4), which can be tuned by solvent polarity. In particular, we demonstrate that the dielectric constant of the electrolyte plays a critical role in modulating the retention time, ranging from rapid ion relaxation to effectively permanent trapping within the crown ether layers. Experimental measurements and density functional theory (DFT) calculations reveal that these parameters reshape the free energy landscape of ion-DC binding versus solvation, thereby tuning the effective k1/k-1 ratio and controlling the rate of ion release. By selecting intermediate solvent conditions, we achieve memory retention dynamics suitable for emulating key short-term and long-term synaptic functions (Fig. 5).

Conclusions and Future Steps:

In conclusion, we constructed a bilayer EGT with a polymeric ion trapping layer to elucidate the molecular origin of ionic retention in such devices. Ion concentration and solvent polarity emerged as critical factors governing the kinetic and thermodynamic control of ionic retention. In particular, the solvent's dielectric constant played a pivotal role in modulating the balance between ion binding to crown ether units and ion solvation, leading to behaviors ranging from effectively permanent trapping to rapid ion relaxation. Intermediate solvent conditions allowed for the emulation of key short-term and long-term plasticity functions, thereby demonstrating a proof-of-concept neuromorphic device. These results highlight key strategies for controlling ion relaxation dynamics, providing valuable insights for the design of ionic–electronic artificial synapses.

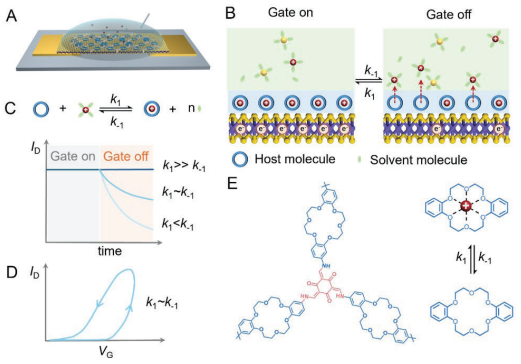

Figure 1: Working mechanism of the hybrid bilayer electrolyte-gated transistor.(A) Schematic of the bilayer transistor.(B) Illustration of ion capture/release in DCP film driven by gate-voltage.(C) A simplified schematic illustrating ion capture/release reaction rates (top), and the effect of these reaction rates on the dynamics of source-drain current (ID) (bottom). (D) Transfer characteristics of the bilayer transistor with comparable ion capture and release rates. (E) Structure of the ion trapping layer functionalized with 18-crown-6 building unit (left), and ion trapping/release reactions with crown ether units

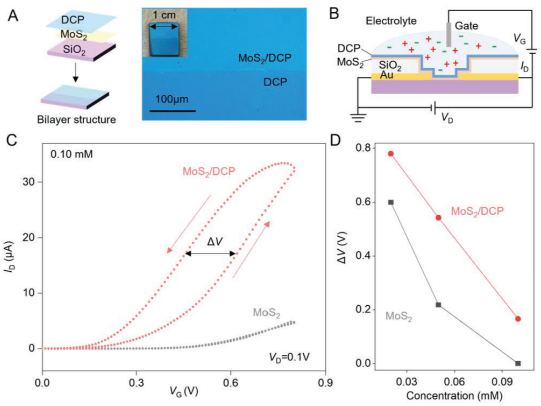

Figure 2: Electrical characterization of the hybrid bilayer electrolyte-gated transistor. (A) Schematic illustration of the stacking of bilayer structure (left) and optical image of the MoS2/DCP bilayer (right). Inset: Photo of the bilayer structure. (B) Schematic of the electrical characterization setup. (C) Transfer characteristics of the MoS2/DCP and MoS2 based transistors. (D) Hysteresis as a function of electrolyte concentration.

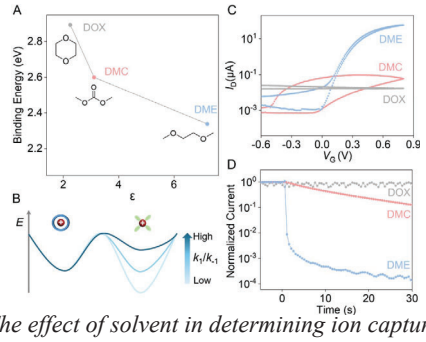

Figure 3: The effect of solvent in determining ion capture/release dynamics. (A)Ion-host binding energy as a function of the solvent's dielectric constant. (B) Energy diagram of the ion-interaction between host molecules and solvate molecules as a function of trapping dynamics. Effect of solvent on (C) the transfer characteristics of the bilayer transistor, and (D) Ion-retention dynamics measured in terms of normalized source-drain current after gate voltage application

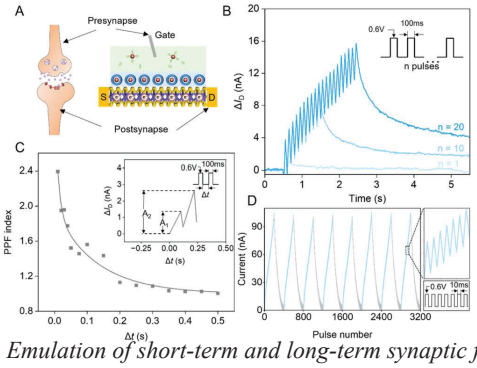

Figure 4: Emulation of short-term and long-term synaptic functions in the bilayer transistor. (A) Schematic illustration of the analogy between a biological neuron and the bilayer transistor (B) Short-term to long-term memory transition induced by the application of many gate pulses. (C) Paired pulse facilitation showing the relative magnitude of current increment as a function of the time-interval between two consecutive gate pulses. (D) Long-term potentiation and depression achieved by the application of a train of gate pulses.

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Imaging Radiation Detectors for Synchrotron X-Ray Sources and Electron Microscopes

CNF Project Number: 306523
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Primary CNF Tools Used: Cadence Virtuoso

Abstract:

Advances in the brilliance of synchrotron x-ray sources and electron microscopes have outpaced the ability of radiation detectors to efficiently capture high-resolution diffraction data. This is especially true for ptychography, a promising method that allows detailed atomic structural determination of samples even for non-periodic samples. Ptychographic diffraction data are characterized by an enormous dynamic range, with low-angle scatter often millions of times more intense than high angle data; both low- and high-angle data are required for ptychographical reconstructions. In consequence, there is need for radiation detectors that can simultaneously capture quantitative images containing very intense low-angle scatter and quantum limited single x-ray or electron data at high angles. Ptychography requires the sequential acquisition of many diffraction patterns to make a full data set; hence, a very fast image frame rate is also required. The goal of our research is to explore detector integrated circuit structures that would allow the fabrication of imaging radiation detectors to meet these challenges.

Summary of Research:

The imaging detectors being explored are Pixel Array Detectors (PADs). PADs consist of a silicon diode sensor array bump-bonded pixel-by-pixel to a pixelated Application Specific Integrated Circuit (ASIC). Each pixel in sensor layer detects incident radiation and produces an electrical signal whose charge is proportional to the integrated x-ray energy. This is conveyed by microlithographic solder connection "bump" to electronics in the corresponding ASIC pixel for processing (Figure 1).

The approach being explored is to advance the charge-pump amplifier arrangement pioneered in our laboratory [1] to provide both sensitivity and dynamic range at higher frame rates than existing detectors. The integrating amplifier that receives the sensor signal must balance two conflicting requirements: It must have a high signal-to-noise ratio for unambiguous detection of single x-ray or electron quanta, thereby requiring a small feedback capacitor to provide high gain. At the same time a large dynamic range dictates use of a large feedback capacitor to integrate the signal from many quanta during an image exposure. The charge-pump circumvents these constraints by preventing the amplifier from reaching saturation. It does this via circuitry that constantly monitors the output of the amplifier. When the amplifier signal approaches saturation, corresponding to integration of many tens or hundreds of radiation quanta, a charge removal circuit is engaged that removes a fixed quantity of charge from the feedback amplifier capacitor and adds a bit to a digital counter. This process occurs without interrupting continued incident charge integration. At the end of the radiation exposure, the digital sum is scaled and added to the digitized value of any signal remaining on the feedback capacitor to provide the total integrated signal.

Research for the current project involved a cycle of redesign, simulation, fabrication, and testing to produce ASIC circuit structures with extended dynamic range, frame rate, and radiation hardness relative to prior designs.

Conclusions and Future Steps:

The next step is to combine the advanced circuits that were studied to produce a miniature detector to test actual radiation imaging performance. This will involve layout and fabrication of a 16x16 pixel test ASIC that will be bump-bonded to a sensor. It will also require the construction of accompanying external readout circuitry, cooling and vacuum housing and development of firmware to coordinate the many signals required to read out an image. This small prototype detector will then be tested for image acquisition performance with x-rays and in an electron microscope.

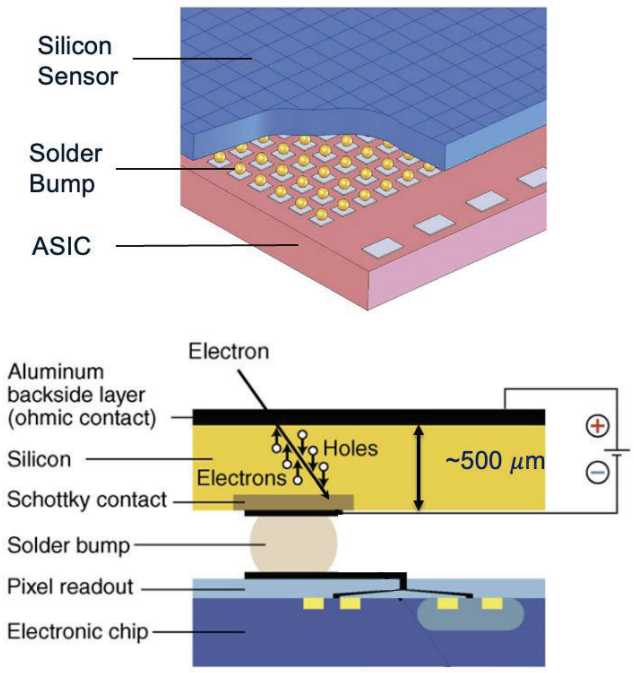

Figure 1: Simplified block diagram of a Pixel Array Detector

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SUPREME Tasks 6/7

CNF Project Number: 307823
Principal Investigator(s): James Hwang
User(s): Yunjiang Ding, Jin Hong Joo, Chunyi Li

Affiliation(s): Department of Materials Science and Engineering, Cornell University

Primary Source(s) of Research Funding: SRC/DARPA

Contact: jch263@cornell.edu

Primary CNF Tools Used: ABM Contact Aligner, SUSS MA6-BA6 Contact Aligner, Unaxis 770 Deep Silicon Etcher, AJA Ion Mill, AJA Sputter Deposition, Veeco Savannah ALD, Electroplating Hood – Au/Cu, P7 Profilometer, Zygo Optical Profilometer,HFTL DC Probe Station, HFTL Small-Signal Probe Station

Abstract:

For heterogeneous integration of millimeter-wave transceiver frontends, we compare the millimeter-wave loss of coplanar interconnects fabricated on Si interposers with different resistivities. Coplanar interconnects 2146-μm long are laid out on two types of Si substrates: HR Si (resistivity > 1 kΩ·cm, thickness = 155 μm) and doped Si (resistivity < 10 Ω·cm, thickness = 205 μm). Small-signal measurements from 1 GHz to 40 GHz indicate the advantages of high-resistivity (HR) Si interposers for heterogeneous integration of millimeter-wave circuits.

Summary of Research:

The width of the center electrode of the coplanar interconnect and its gap to the ground electrode are 30 μm and 16 μm, respectively, resulting in a characteristic impedance ≈ 50 Ω. The ground electrodes are grounded by a high density of through-silicon vias (TSVs) to suppress higher-order modes. To mitigate the residual stress from thermal expansion mismatch, TSVs are metallized with Al having an annular structure (Fig. 1) [1]. Front-side wafer fabrication comprises mainly sputtering of 20-nm Ti and 1.5-μm Al and patterning by liftoff. The most critical steps of backside fabrication involve etching and metallizing 50-μm-diameter TSVs. Using the Bosch process [2] with a 200-nm Al2O3 hard mask, the substrates are deep etched from the backside at an etch rate of 27 nm/s. TSV metallization is then carried out by depositing 50-nm Pt using atomic layer deposition [3], followed by 70-nm Ti and 2-μm Al using sputtering (Fig. 2) [4]. DC measurements confirm a TSV series resistance on the order of 1 Ω. Small-signal millimeter-wave on-wafer measurements (Fig. 3) show the coplanar interconnect fabricated on HR Si have an insertion loss of 0.7 dB/mm at 40 GHz (Fig. 4), an order of magnitude better than the same coplanar interconnect fabricated on doped Si. The return loss of the coplanar interconnect fabricated on HR Si is always greater than 20 dB between 1 and 40 GHz.

Conclusions and Future Steps:

The above result confirms that it is necessary to use HR Si (as opposed to doped Si) as an interposer for heterogeneous integration of millimeter-wave transceiver frontend. In the future, HR Si of different resistivities will be compared to determine the optimum resistivity level.

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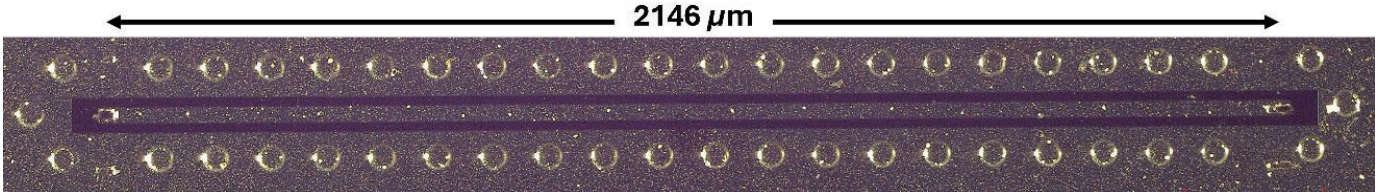

Fig. 1. Micrograph showing a 2146-μm-long grounded coplanar interconnect within two parallel rows of TSVs to prevent higher-order modes from propagating.

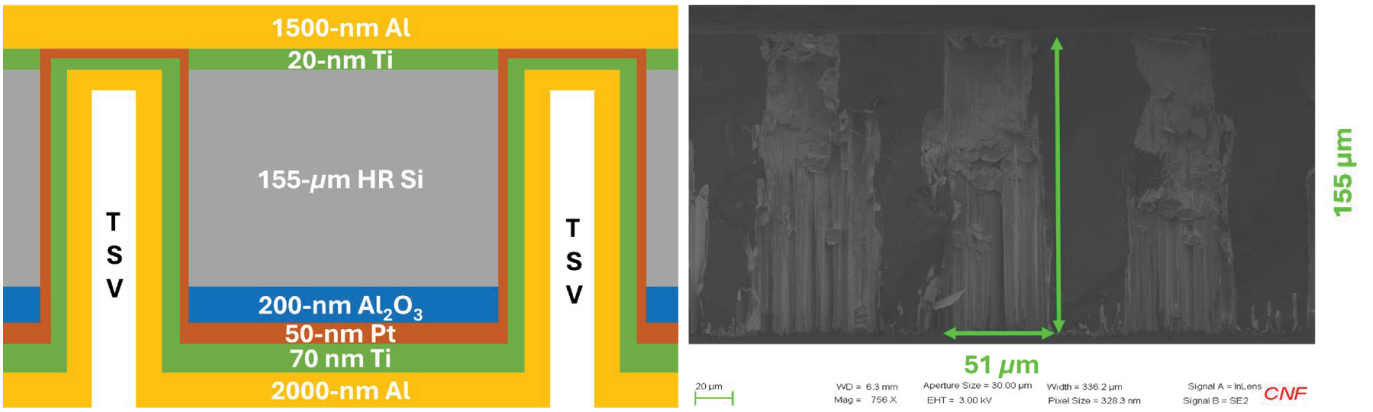

Fig. 2. Cross-section (a) schematic and (b) SEM image of a metallized through-Si via (TSV).

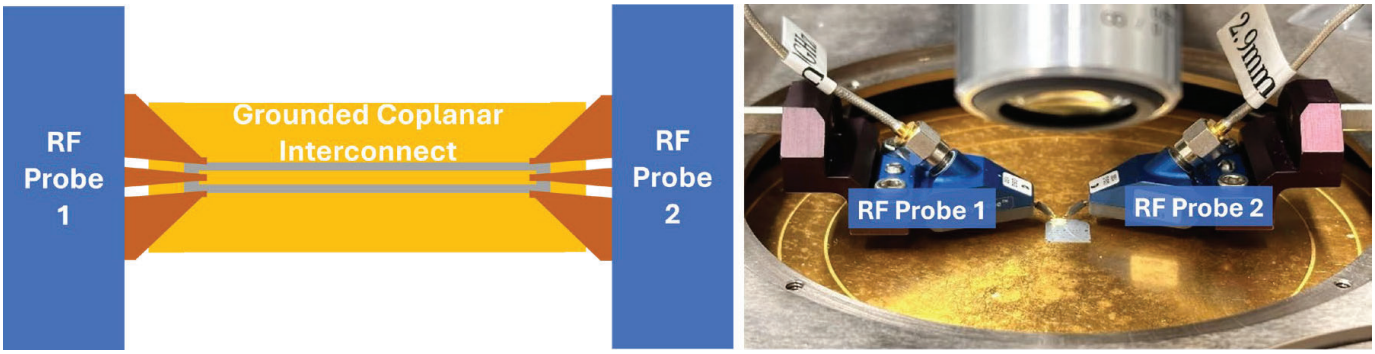

Fig. 3. (a) Schematic and (b) photograph of coplanar interconnect under millimeter-wave test.

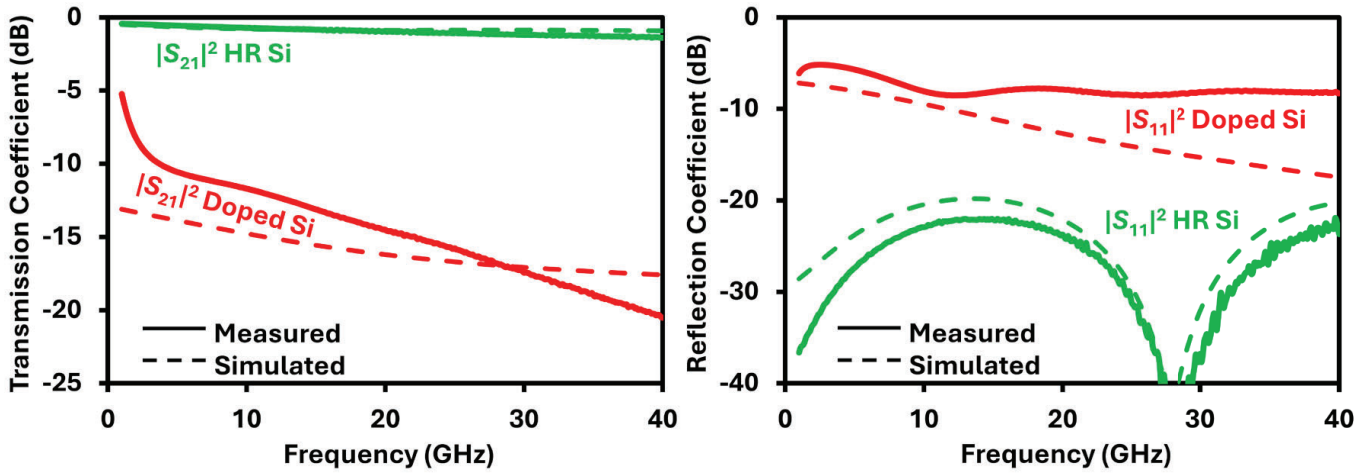

Fig. 3. (a) Schematic and (b) photograph of coplanar interconnect under millimeter-wave test.

Nanoelectronic Artificial Intelligence Processors

CNF Project Number: 316924
Principal Investigator(s): Peter McMahon
User(s): Guilherme Marega, Ruomin Zhu, Yongqi Zhang

Affiliation(s): Applied & Engineering Physics department, Cornell University

Primary Source(s) of Research Funding: the David & Lucile Packard Foundation, Cornell AEP

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Website: https://mcmahon.aep.cornell.edu/index.html

Primary CNF Tools Used: Westbond 7400A Ultrasonic Wire Bonder, KLA P7 Profilometer, YES EcoClean Asher, Oxford 81 RIE, Suss MA6|BA6 Aligner, Hamatech Hot Piranha, Oxford PECVD, Oxford 100 ICP Dielectric, Woollam RC2 Spectroscopic Ellipsometer, Zeiss Ultra SEM, Oxford 82 RIE

Abstract:

Resistive crossbar arrays co-locate memory and analog computation to overcome the von Neumann "memory wall," where data movement can dominate energy costs. By encoding weights in multi-level resistive cells and performing parallel dot-product operations directly within a 16 × 16 array fabricated at the Cornell Nanoscale Facility, we demonstrate up to 60.9 TOPS/W and four decades of linear dynamic range [1]. This in-memory computing platform offers a compelling path toward dramatically lower-power AI inference, as well as efficient signal and image processing.

Summary of Research:

The explosive growth of AI services is driving data-center electricity demand toward unsustainable levels. The International Energy Agency projects global data-center energy use to exceed 945 TWh by 2030—more than double current levels—and U.S. data centers, already consuming 4.4 % of national electricity in 2023, may account for up to 12 % by 2028 [4][5]. Even a single Artificial Intelligence query carries a measurable footprint: a typical ChatGPT interaction consumes roughly 0.3 Wh, equivalent to running an LED bulb for several minutes [6].

Conventional von Neumann architectures exacerbate this burden via the "memory wall," in which moving a 64-bit word from Dynamic Random Access Memory (DRAM) to the Central processing unit (CPU) costs on the order of 1,000 pJ—about 50× the energy of a 64-bit floating-point add [7]. Across real workloads, data transfers can account for 60–70 % of total system energy, severely limiting both performance and efficiency.

Resistive crossbar arrays address this challenge by performing matrix-vector multiplications in situ: voltages applied to row lines induce column currents proportional to conductance-encoded weights, realizing massively parallel dot products in one step. Hardware demonstrations include 60.9 TOPS/W for binary neural inference in oxide-based devices [1], 405 TOPS/W in magnetoresistive prototypes at 0.8 V [2], and 3.6 TOPS/W in designs with nonlinear Analog Digital Converters (ADCs) for specialized preprocessing [3].

Since the first memristor crossbar proposal in 2008, the field has advanced rapidly: writes as low as 6 fJ per cell for sparse coding [8], 24 TOPS/W in XNOR-RRAM arrays monolithically integrated with 90 nm CMOS [9], and area efficiencies exceeding 130 TOPS/mm² alongside the aforementioned TOPS/W milestones [2].

In our work, we aim to fabricate resistive crossbar arrays with AI model encoded on them to save energy for AI computing. As a first step, we have fabricated 16 × 16 arrays using a CMOS-compatible process and measured their analog performance at Cornell Nanoscale Facility. By encoding image-processing kernels as conductance matrices and feeding input voltages corresponding to grayscale images, we obtained output currents that reproduce digital convolution outputs with high fidelity (Fig. 4), validating hardware-in-the-loop processing as a viable digital alternative.

Conclusions and Future Steps:

We have shown that resistor-based crossbar arrays can achieve state-of-the-art energy efficiency for low-precision AI and image-processing tasks. To scale this approach, we plan to:

- Increase array dimensions from 16 × 16 to 128 × 128, enabling higher-resolution kernels and larger neural-network layers.

- Expand application domains to voice-signal processing, discrete Fourier transforms and AI computing, leveraging the same in-memory dot-product primitive.

These developments will bring in-memory computing closer to deployment in edge AI accelerators and high-

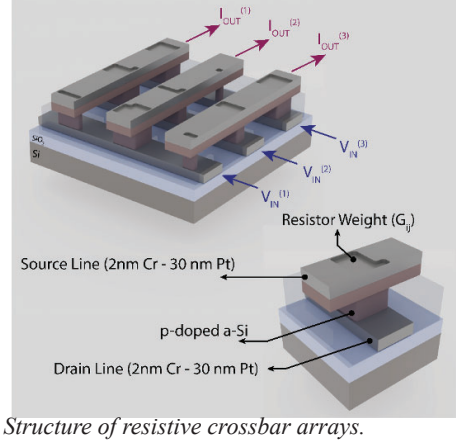

Figure 1: Structure of resistive crossbar arrays.

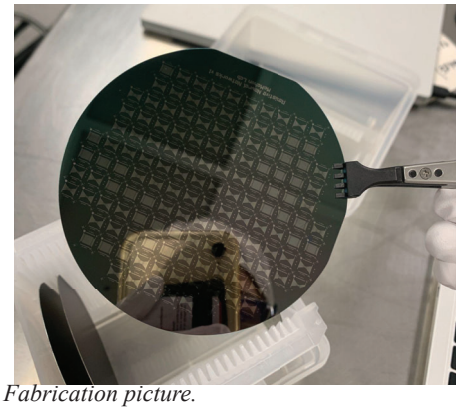

Figure 2: Fabrication picture.

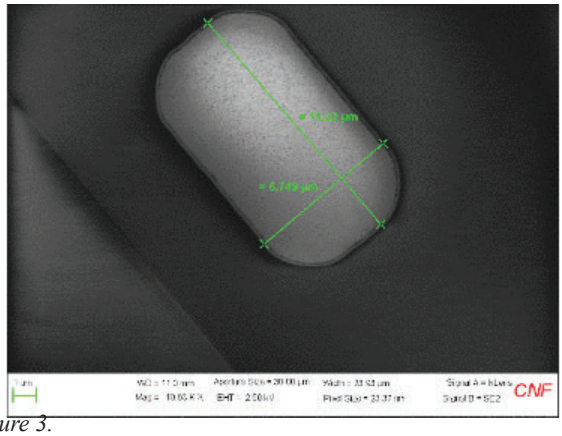

Figure 3.

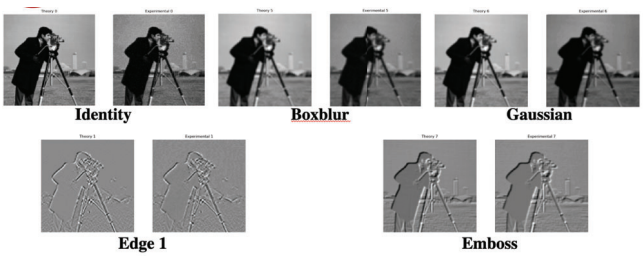

Figure 4: Digital and Hardware processing results.

throughput signal-processing hardware.

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Validation of a First Digitho Programmable Photomask Prototype

CNF Project Number: 318324
Principal Investigator(s): Richard Beaudry
User(s): Guilherme Marega, Richard Beaudry

Affiliation(s): Digitho Technologies inc.

Primary Source(s) of Research Funding: NRC-IRAP, private funds and Fabric Program from ISED

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Primary CNF Tools Used: GCA 5X g-line Stepper, GCA AS200 i-line Stepper

Abstract:

This report outlines the validation of a novel programmable photomask concept leveraging liquid crystal display (LCD) technology for dynamic UV lithography. Conducted at the Cornell NanoScale Facility, the evaluation focused on assessing the system's compatibility with standard g-line and i-line steppers, as well as its ability to support reconfigurable exposure processes. The results highlight the potential of LCD-based photomasks to serve as flexible, low-cost alternatives to conventional chrome masks, opening pathways for rapid prototyping and adaptive lithographic workflows in microfabrication.

Summary of Research:

The growing demand for reconfigurable and cost-effective lithographic tools has prompted exploration of alternatives to static, photolithography-grade chrome masks. In this context, the programmable photomask evaluated in this project integrates an LCD panel capable of modulating UV light in real time, combined with an embedded photodiode for synchronized exposure control. This approach seeks to enable dynamic patterning, reduce reliance on mask fabrication cycles, and facilitate multi-step or adaptive processes within research and development environments. An overview of the photomask structure and components is provided in Figure 1.

The prototype was tested using both g-line and i-line stepper systems at CNF to determine its operational compatibility with established lithography platforms. These tests demonstrated that the system could be integrated without requiring modification to tool workflows or introducing risk to equipment. The ability to maintain wireless communication and reliably update displayed images in response to UV exposure pulses marks a key step toward practical deployment in cleanroom settings.

In addition to confirming mechanical and communication compatibility, the campaign evaluated the core optical performance of the mask with the g-line stepper. Measurements confirmed sufficient UV transmittance (~20% for white pixels, 6–8% for black pixels) and contrast (>60%) for lithographic patterning, with successful image cycling and exposure repeatability demonstrated on resist-coated wafers. Results from these exposure tests are illustrated in Figure 2, while microscopy analysis of the patterned resist confirms a minimum resolved feature size below 100 μm, as shown in Figure 3.

The system also showed the ability to perform basic grayscale patterning through modulated exposures, reinforcing its suitability for early-stage prototyping and multi-depth resist structuring. These findings position LCD-based programmable photomasks as promising enablers of adaptable lithography workflows, with ongoing improvements aimed at enhancing resolution, synchronization robustness, and spectral compatibility.

Conclusions and Future Steps:

The successful validation of the LCD-based programmable photomask under real-world lithographic conditions marks a promising step toward more agile and cost-efficient fabrication workflows. By demonstrating compatibility with both g-line and i-line steppers, maintaining stable wireless communication, and delivering consistent image cycling during UV exposures, this system underscores the feasibility of deploying reconfigurable photomasks in advanced microfabrication environments.

While the current implementation relies on an LCD panel, which is limited to g-line and unsuitable for i-line exposure due to its lack of transparency below 400 nm, future versions of the system are expected to incorporate MEMS-based modulators. These alternatives offer the potential for higher optical performance, broader spectral compatibility—including true i-line transparency—and

improved spatial resolution. Such advances would enable programmable photomasks to reach application domains currently limited to traditional chrome masks.

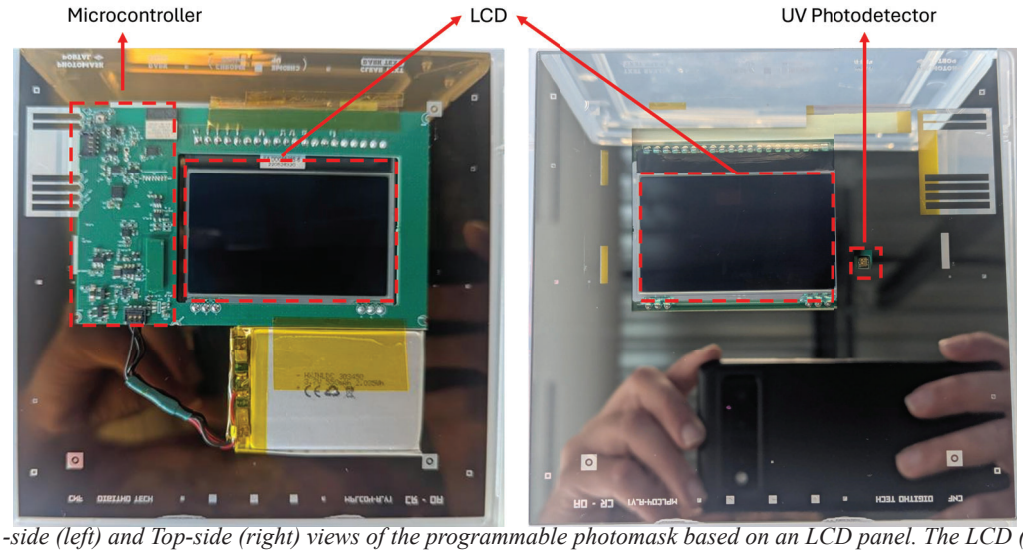

Figure 1: Bottom -side (left) and Top-side (right) views of the programmable photomask based on an LCD panel. The LCD (central red box) modulates UV light during exposure, while the integrated photodiode (rightmost red box) detects UV flashes to trigger image updates. The Bottom side includes control electronics and a rechargeable battery for wireless operation.

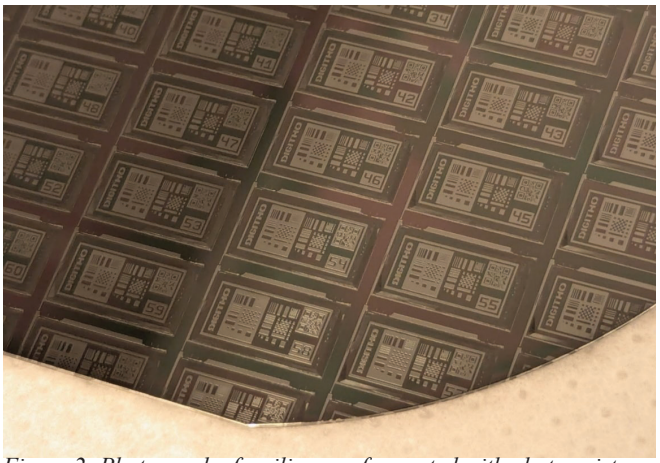

Figure 2: Photograph of a silicon wafer coated with photoresist and exposed using the programmable LCD photomask. Each rectangular field corresponds to a different image in the programmed sequence, demonstrating successful image cycling and pattern transfer during exposure.

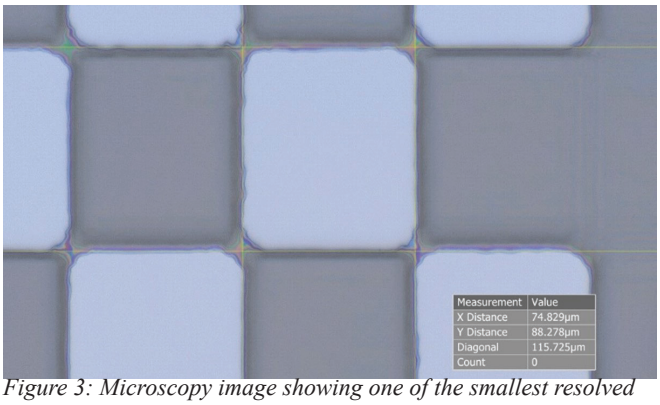

Figure 3: Microscopy image showing one of the smallest resolved features obtained using the programmable photomask. The measured dimensions are approximately 74.8 µm × 88.3 µm, confirming lithographic resolution below 100 µm consistent with LCD pixel limitations.

Microchannel Fabrication on Silicon Wafer and Development of Heating Elements on Silicon and Sapphire

CNF Project Number: 319424
Principal Investigator(s): Srikanth Rangarajan
User(s): Pranay Nirapure

Affiliation(s): Binghamton University

Primary Source(s) of Research Funding: National Science Foundation, Semiconductor Research Corporation

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Primary CNF Tools Used: Lesker PVD75 Sputter, CVC SC4500 Odd-hour evaporator, MRL A1 General Anneal

Abstract:

This project reports on the fabrication and post-deposition treatment of a transparent heater using a 600 nm thick Indium Tin Oxide (ITO) film sputtered onto a sapphire substrate. Following ITO deposition, a thin metal contact layer composed of 2 nm titanium and 150 nm gold was evaporated to facilitate electrical probing. ITO was deposited using the Lesker PVD 75 sputtering tool at 100 degrees Celsius, and post-annealing was conducted in ambient air at 500 degrees Celsius for 45 minutes. The device is designed to retain high optical transmittance while enabling Joule heating and low-resistance contact.

Summary of Research:

The objective of this project was to develop a transparent, electrically conductive heater using ITO on a sapphire substrate, integrated with metal contacts for reliable electrical interfacing. Transparent heaters are essential to study the bubble nucleation in boiling phenomena. Transparent heaters allow for both optical access and local heating, making them ideal for this study.

Sapphire substrates were selected for their desirable thermal properties, along with optical clarity and mechanical robustness. ITO was chosen as the heater material due to its high transmittance in the visible spectrum and relatively desirable sheet resistance when properly processed.

The ITO layer was deposited using the Lesker PVD 75 RF magnetron sputtering system. Deposition was carried out at a substrate temperature of 100 degrees Celsius under an argon ambient. The resulting film thickness was 600 nanometers.

Post-deposition annealing trials are being conducted in ambient air to improve crystallinity, reduce resistivity, and maintain high optical transmission. Annealing is to be performed in a tube furnace at 400 degrees Celsius for 45 minutes. This air anneal condition is supposed to provide a good balance between transmittance and electrical performance. While forming gas anneals can further reduce sheet resistance, they were not used in this iteration.

To enable low-resistance electrical contacts, a bi-layer metal stack was deposited using the CNF Odd-Hour. A 2 nm titanium adhesion layer was deposited directly on the ITO, followed by 150 nm of gold. Titanium provides good adhesion to both ITO and the underlying sapphire, while gold serves as a chemically inert, low-resistance contact layer suitable for wire bonding or probing.

The annealed ITO films exhibited an estimated average visible transmittance of 80 to 85 percent, with peak transmittance near 550 nanometers. The sheet resistance was estimated to be between 10 and 15 ohms per square, depending on grain structure, carrier mobility, and stoichiometry. These values are within expected ranges for ITO processed under similar conditions. [1] [2] [3]

The completed heater consists of a transparent region for optical access and well-defined metal pads for electrical interfacing, please refer to Fig. 1. The heater is compatible with applications requiring simultaneous thermal and optical functions. Future work will include photolithographic patterning of heater geometries and optimization of contact pad layouts.

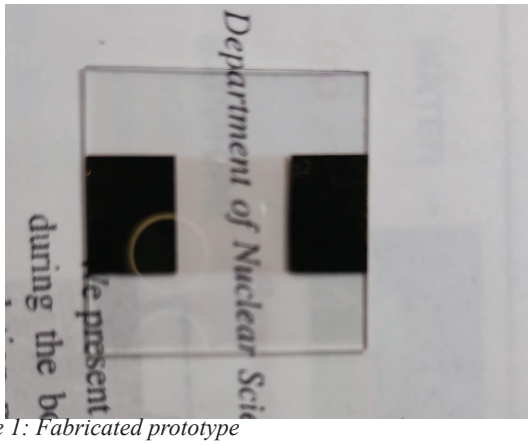

Figure 1: Fabricated prototype

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Interconnect-Based Temperature Sensing Array for IC Thermal Management

CNF Project Number: 321024
Principal Investigator(s): Ping-Chuan Wang and Graham Werner
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Primary Source(s) of Research Funding: SUNY New Paltz Research and Creative Projects Award (RCPA)

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Primary CNF Tools Used: Heidelberg MLA 150, Hamatech Wafer Processor, CVC SC4500 Odd-hour evaporator, YES EcoClean Asher Filmetrics Reflectometer

Abstract:

Excessive self-heating in integrated circuits (ICs) is a major barrier to performance and reliability within the semiconductor industry and necessitates innovation in thermal management [1,2], prompting detailed measurements of IC temperature with adequate spatial and temporal resolutions in designing and characterizing innovative cooling devices. This project presents the fabrication of an in-line spatial and temporal temperature mapping system designed to interface directly between an IC and its cooling device, consisting of a dense array of 64 aluminum Resistance Temperature Detector (RTD) sensors. The RTD array was successfully fabricated at CNF using a single-layer lift-off process on an oxide-coated silicon wafer, before integration into a measurement system. Our project validates the design, fabrication, and characterization of an aluminum RTD sensor array system for in-situ, high resolution thermal mapping, contributing to the experimental evaluation of IC thermal management solutions.

Summary of Research:

Resistance Temperature Detectors (RTDs) were chosen due to their straightforward device physics, use of a single conventional conductor, and fabrication simplicity through a single lithography step [3,4]. The RTD structure consisted of 64 individual serpentine-pattern sensors, spaced evenly to cover a 25 mm x 25 mm sensing area (Figure 1), with two arrays fabricated on a single 4-inch wafer. Fabrication employed a lift-off process on silicon wafers first passivated with thermally grown SiO2 (Figure 2). A bi-layer of lift-off resist and positive tone photoresist were spin-coated before pattern development. The Heidelberg MLA 150 maskless direct-write tool was used to expose the RTD design. The exposed photoresist was then developed in a Hamatech-Steag wafer processor, followed by dry-oxygen plasma descum using an Anatech plasma asher to remove resist residues.

Following development, metallization was performed, where A 100 Å titanium adhesion layer was followed by deposition of 2000 Å of aluminum using electron beam physical vapor deposition (EB-PVD). Lift-off was performed with an automated tool, and SiO2 passivation was applied atop metal pattern using PECVD after optimizing pre-cleaning to avoid damage to the aluminum, providing necessary electrical and mechanical insulation. After dicing and packaging, the calibrated system performed real-time measurements by multiplexing continuously across the sensor array to perform 4-point resistance measurements.

Once calibrated, the sensor array showed minimal sensor-to-sensor temperature variation under ambient conditions, with 0.18% variability at room temperature. During thermal transients, spatial temperature variations were resolved within 0.1 °C.

Conclusions and Future Steps:

The fabricated RTD sensor array successfully demonstrated ambient and transients with suitable spatiotemporal resolution for non-uniform thermal gradients during heating and cooling cycles. The measured average sensitivity was 0.197 ± 0.004 mV/°C, consistent with design expectations. Limitations include aluminum's inferior thermal properties compared to platinum for RTDs, and a lower spatial resolution of 10 sensors/ cm², which may be insufficient in some applications. Future work will focus on validating the system through numerical modelling or thermal finite element analysis (FEA) to ensure accuracy in detecting spatial temperature variations.

References:

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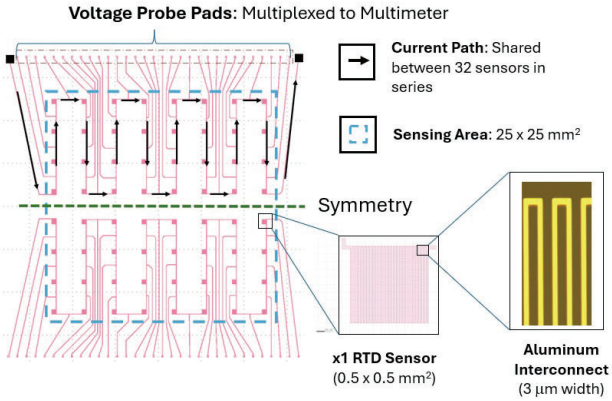

Figure 1: Layout of RTD sensor array.

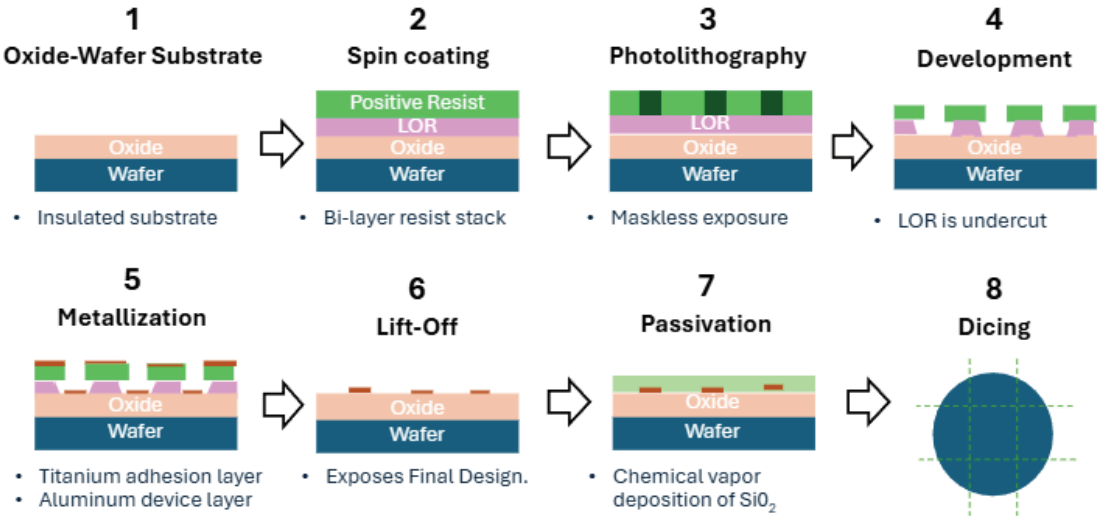

Figure 2: Lift-off fabrication steps.

Aluminum CMP Planarization for Graphene FETs

CNF Project Number: 321524
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User(s): William Huang

Affiliation(s): Department of Microsystems Engineering, Rochester Institute of Technology, Department of Electrical and Microelectronics Engineering, Rochester Institute of Technology.

Primary Source(s) of Research Funding: Rochester Institute of Technology

Contact: ixpeme@rit.edu

Primary CNF Tools Used: Logitech Orbis CMP / Aluminum

Abstract:

As silicon CMOS technology approaches its scaling limits, graphene offers a compelling alternative due to its high carrier mobility, atomically thin profile, offering strong electrostatic control and promising high-frequency performance. However, roadblocks such as device-to-device variation, high contact resistance, poor dielectric interfaces, and non-uniform graphene quality have limited the adoption of graphene field - effect transistors (GFETs). In this work, we directly compare two GFET structures through a controlled, side-by-side process split to evaluate the impact of gate electrode topography (raised vs. recessed buried local gate) in terms of device performance and device-to-device variation. While the top performing devices remained similar across the three proposed structures, very significant differences are seen in terms of yield and device-to-device variation in the proposed variations. The device-to-device variation of the hole mobility dropped from 36% to 19%, device yield increased from 54.4% to 65.1%, Dirac voltage was reduced from 1.2 V to 0.7 V when a recessed local-back gate is used as opposed to a raised local-back gate. As such, this study shows that a direct comparison of process conditions can help identify favorable process conditions to improve the manufacturability of graphene-based transistors.

Summary of Research:

The integration of a planarization process for the fabrication of GFETs with hBN dielectrics, results in both a smoother transition from channel to gate as shown in schematically in Figure 1, and Figure 2. The planarization process provides a statistical improvement in the performance and variability of graphene transistors in terms of Dirac point and mobility when compared to a raised gate architecture as shown in Figure 3 and Figure 4. Hysteresis measurements (not shown) also indicate that the level of traps in the hBN/graphene interface is similar between the raised and recessed process. When compared to other dielectrics such as Al2O3 [1], hBN also offers advantages in terms of yield and contact resistance when used in a local-back gate process. In addition, the observed parameter variability is much reduced with the use of hBN as a dielectric due to better material compatibility during processing, which along with other process improvement and considerations, could lead to the needed improvement in yield and reliability [2], [3], [4]

Conclusions and Future Steps:

While prior studies have aimed to improve GFET performance or reduce variability, most work has typically done so in evaluating disparate device structures, materials, or fabrication flows, and focusing only on "hero" devices that do not reflect broader statistical trends. In contrast, our work systematically integrates monolayer hBN as a gate dielectric and a CMP-recessed aluminum gate within a unified fabrication platform, enabling direct, controlled comparisons across design variations. This approach not only enhances key performance metrics, such as contact resistance, mobility, and cutoff frequency, but also dramatically reduces device-to-device variation and increases yield. By analyzing full device distributions rather than peak values alone, this study offers critical insights into how dielectric choice and gate geometry together influence reproducibility. Demonstrating a substantial reduction in device variability, the standard deviation of extracted hole mobility decreased from 36% to 18%, while device yield improved significantly from 54.4% to 65.1%. The Dirac point shifted closer to 0 V (from ~1.2 V to 0.7 V), and the contact resistance was reduced from 0.75 kΩ to 0.67 kΩ. Ultimately, our findings establish practical design and process guidelines for realizing scalable, high-performance graphene electronics to bridge gaps between isolated breakthroughs and manufacturable, wafer-level technologies. The reduction in device-to-device variation indicates that a process induced variation may be mitigated through the presented work.

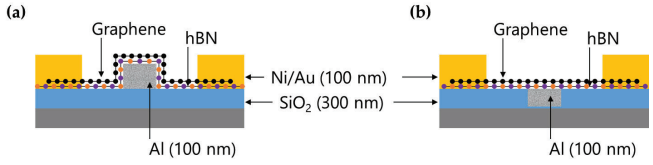

Figure 1: Device cross-section for (a) raised Al gate with hBN gate dielectric and (b) recessed Al gate with hBN gate dielectric.

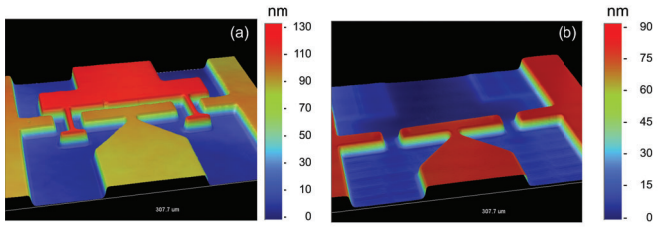

Figure 2: Three-dimensional white light interferometry scans of fabricated (a) raised and (b) recessed Al/hBN/graphene field effect transistors.

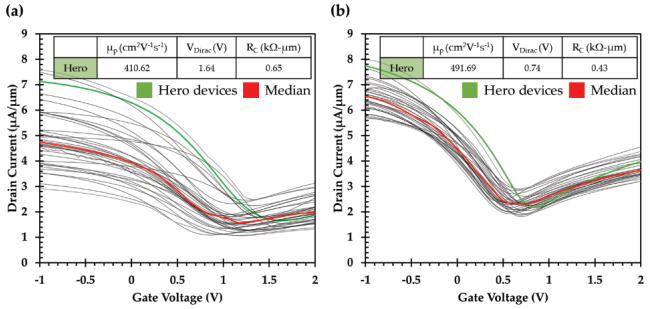

Figure 3: Transfer characteristics overlay at VDS = 0.1 V of fabricated graphene FETs with a gate length of 10 μm drain current normalized to its width of 20 μm and contact resistance (RC) normalized to its width (a) raised Al gate with monolayer hBN gate dielectric and (b) recessed Al gate with monolayer hBN gate dielectric.

The finding implies that extending the process flow to further large-scale integration may support a more uniform device array and a scalable, multi-user circuit design platform. By analyzing full device distributions rather than peak metrics alone, this study reveals how dielectric selection and gate geometry directly influence reproducibility. The observed consistency suggests that this hBN/ recessed gate structure is a strong candidate for an optimal platform of scalable, and high-performance GFET fabrication.

References:

[1] T. J. Huang, A. Ankolekar, A. Pacheco-Sanchez, and I. Puchades, "Investigating the Device Performance Variation of a Buried Locally Gated Al/Al2O3 Graphene Field-Effect Transistor Process," Applied Sciences (Switzerland), vol. 13, no. 12, Jun. 2023, doi: 10.3390/app13127201.

[2] S. Fukamachi et al., "Large-area synthesis and transfer of multilayer hexagonal boron nitride for enhanced graphene device arrays," Nature Electronics 2023 6:2, vol. 6, no. 2, pp. 126–136, Feb. 2023, doi: 10.1038/s41928-022-00911-x.

[3] W. Zheng, "Scalable Production of Two-Dimensional Materials Based Microchips Containing Highly-Reliable Transistors," 2025. Accessed: Jul. 24, 2025. [Online]. Available: http://hdl.handle.net/10754/705175

[4] "IRDSTM 2023: Beyond CMOS and Emerging Materials Integration - IEEE IRDSTM." Accessed: Jul. 24, 2025. [Online]. Available: https://irds.ieee.org/editions/2023/20-roadmap-2023-edition/126-irds%E2%84%A2-2023-beyond-cmos-and-emerging-materials-integration

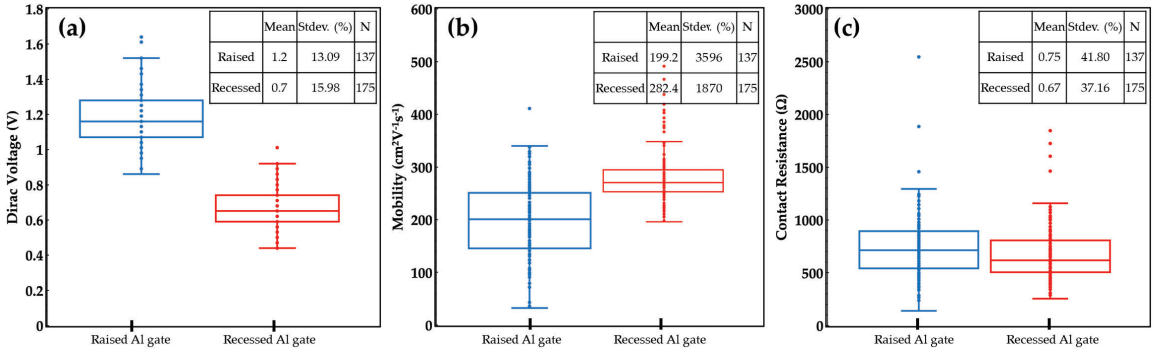

Figure 4: Box and whisker comparison of performance and variation of fabricated devices with raised and recessed aluminum gates in relation to (a) mobility, (b) Dirac voltage, and (c) contact resistance. Within each box and whisker plots, inset indicate the average, % standard deviation and number of working devices for each group.

GALLO

CNF Project Number: 323825
Principal Investigator(s): Jon McCandless
User(s): Kazuki Nomoto

Affiliation(s): Gallox Semiconductors Inc.

Primary Source(s) of Research Funding: National Science Foundation, Breakthrough Energy

Contact: jon@galloxsemi.com

Primary CNF Tools Used: GCA AutoStep 200 DSW i-line stepper, JEOL 6300 E-beam, SEM, PT770 etcher, O2 Asher, Oxford RIE Etcher, AJA sputter system, E-beam evaporator, Oxford PECVD, RTA AG610

Abstract:

Gallium oxide (Ga_2O_3), an ultra-wide bandgap semiconductor, offers strong potential for highpower, high-voltage power electronics due to its large bandgap and high critical electric field strength. This research focuses on the design, fabrication, and testing of Ga_2O_3)-based diodes and transistors, with iterative improvements guided by performance data. Current efforts emphasize electric field management and thermal mitigation to enhance device performance and support future commercialization.

Summary of Research:

Gallium oxide (Ga_2O_3) is an ultra-wide bandgap (~4.8 eV) semiconductor [1]. Its large bandgap and high critical electric field strength make it well suited for high-power, high-voltage power electronics applications [2].

To commercialize Ga_2O_3-based transistors and diodes, devices must be carefully designed, fabricated, and tested. Effective electric field management and thermal mitigation strategies are essential to achieving the material's full potential.

We have designed, fabricated, and tested both diodes (Fig. 1) and transistors (Fig. 2) to evaluate the device performance (Fig. 3), and we continuously iterate: fabrication, testing, and data analysis to inform subsequent design improvements.

Conclusions and Future Steps:

We are working to introduce additional electric field management strategies, and to implement efficient heat removal strategies.

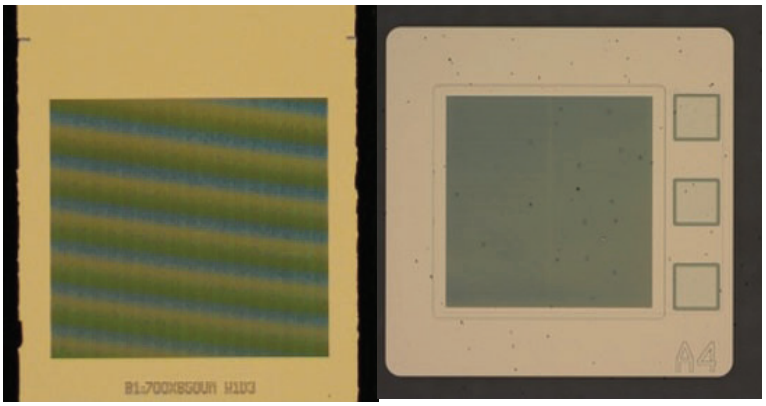

Fig. 1 (Left). A Schottky barrier diode is shown. Fig. 2 (Right). A field effect transistor is shown.

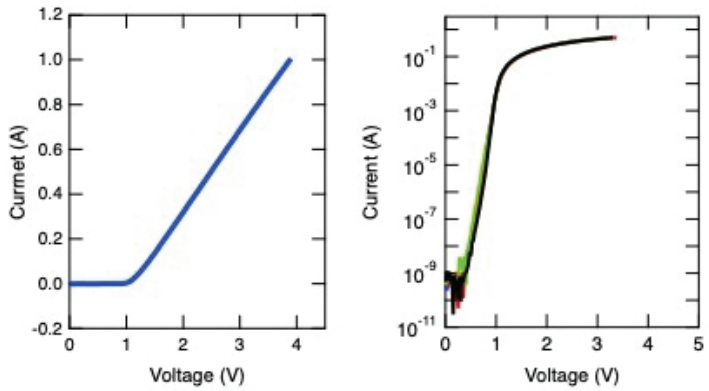

Fig. 3. Schottky barrier diode performance is characterized, and performance is assessed in order to optimize and iterate on the devices design. Current vs voltage measurements are obtained and plotted on a (left) linear scale and (right) log scale.

References:

[1] T. J. Huang, A. Ankolekar, A. Pacheco-Sanchez, and I. Puchades, "Investigating the Device Performance Variation of a Buried Locally Gated Al/Al2O3 Graphene Field-Effect Transistor Process," Applied Sciences (Switzerland), vol. 13, no. 12, Jun. 2023, do

Circuit Integration and Chip Design

CNF Project Number: 325925
Principal Investigator(s): Dr. Younes Ra'di
User(s): Pardha Sourya Nayani, Morteza Moradi

Affiliation(s): Department of Electrical Engineering and Computer Science, Syracuse University, Syracuse, NY, USA

Primary Source(s) of Research Funding: Syracuse University

Contact: yradi@syr.edu

Primary CNF Tools Used: Heidelberg MLA150 MasklessAligner, SC4500 Odd-Hour Evaporator, DISCO Dicing Saw and Westbond 7400A Ultrasonic Wire Bonder

Abstract:

This project focused on the design, fabrication, and testing of a compact circuit integrated into a packaged chip, optimized for impedance behavior analysis. The circuit, composed of capacitors, inductors, and resistors, was carefully designed and laid out for on-chip integration. The inductors were implemented using meander line structures, while the capacitors were realized as interdigitated fingers, together replicating the desired impedance characteristics. The fabricated chips are currently in the testing phase.

Summary of Research:

In this research, we developed a new circuit model consisting of capacitors, inductors, and resistors, which when configured as shown in Fig. 1a produce a desired impedance profile. The initial stage of the project involved theoretical analysis to extract the target circuit parameters, including the required capacitance, inductance, and resistance values. Subsequently, the focus shifted to translating these theoretical values into a practical layout by designing the individual passive components. Rather than designing the complete circuit in a single step, we adopted a modular approach: capacitors and inductors were designed separately and later integrated and optimized to match the desired impedance response. The layout designs were carried out using Keysight ADS, where we explored various geometries and material configurations. Specifically, capacitors and inductors were designed with different dimensions and using various metal layers, such as gold and aluminum, to achieve the same target values. Finally, the individual components were integrated into a complete layout, and the design was optimized to ensure that the overall impedance closely matched the theoretical predictions. The finalized designs were then exported as GDS files, ready for fabrication as seen in Fig. 1b.

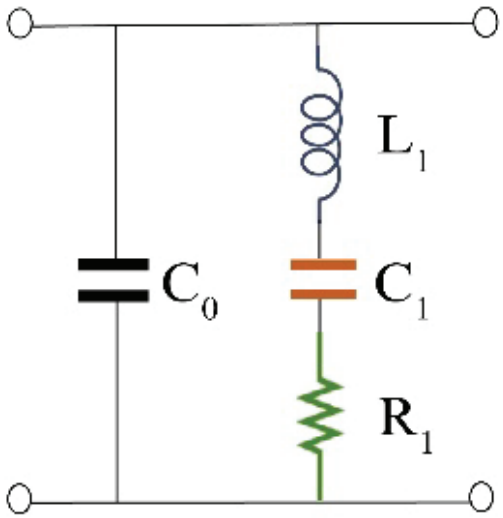

Figure 1a Topology of designed circuit.

At CNF, the fabrication process began with the selection of a 100 mm, prime-grade, n-type silicon wafer. Standard photolithography steps were followed, starting with spin-coating the wafer with a positive photoresist. Maskless lithography was then performed using the Heidelberg MLA 150 system, which enabled direct laser exposure of the desired pattern onto the photoresist without the use of a physical mask. Following exposure, the wafer was developed using an appropriate solvent, resulting in the transfer of the designed pattern onto the photoresist layer. After development, a metal deposition was carried out using the SC4500 Odd-Hour Evaporator. Two different metal stacks were deposited on separate wafers: one with a 1 μm-thick gold layer and the other with a 100 nm-thick aluminum layer. Upon completion of metal deposition, the wafers underwent a lift-off process (refer to Fig. 2a and 2b) to remove the remaining photoresist and define the final patterned metal structures. After the metal deposition and completion of the lift-off process, the wafer was diced into individual dies corresponding to the various unit cell designs developed during the initial design phase as seen in Fig. 3a. These discrete unit cell dies

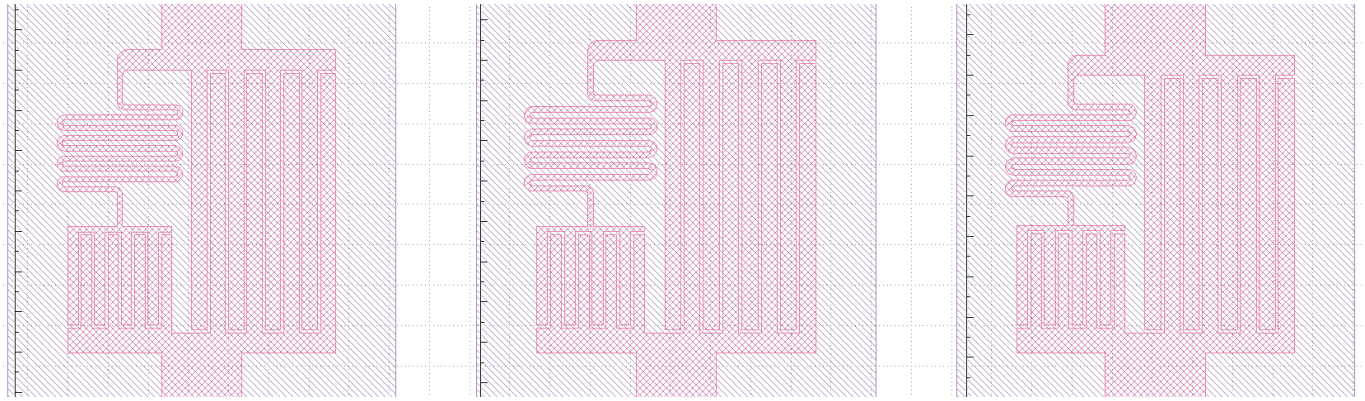

Figure 1b Layout of three different designs.

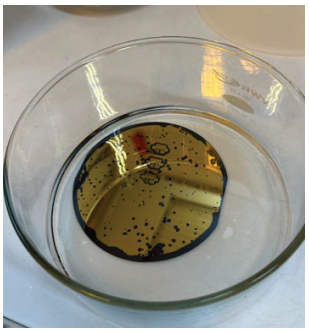

Figure 2a Lift-off process.

Figure 2b Wafer after Lift-off with designed metallic patterns.

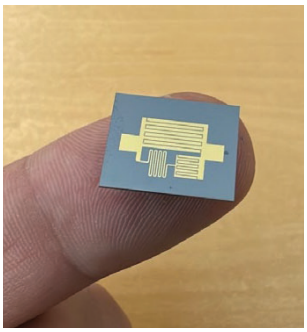

Figure 3a Diced unit cell.

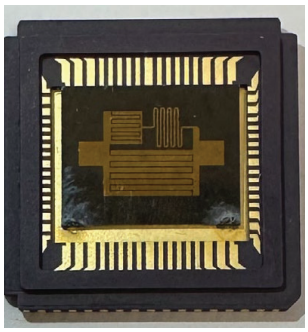

Figure 3b The fabricated circuit in a package.

were subsequently mounted and wire-bonded onto chip carriers for packaging shown in Fig. 3b. The packaged devices are currently in the final stages of preparation for preliminary measurements. We will characterize the fabricated devices by extracting key parameters such as S-parameters and impedance (Z) parameters, and compare the measured data against theoretical predictions. Based on any observed discrepancies, we will iteratively refine the initial designs and adjust intermediate fabrication steps to optimize performance. This cycle of design, fabrication, measurement, and analysis will be repeated until the desired device specifications are met.

Conclusions and Future Steps:

Based on the measurement results obtained, we will fine-tune specific design parameters to enhance alignment with theoretical predictions. Thus far, we have successfully designed and fabricated a single-order circuit unit cell. Moving forward, we plan to extend this work by developing and vertically stacking multiple unit cells to realize higher-order circuit architectures, which will also be fabricated on-chip. This work establishes a systematic design-to-fabrication workflow for custom impedance-engineered circuits at the microscale. The approach enables rapid prototyping and experimental validation of novel circuit topologies directly in integrated form. As the project progresses, further optimization and scaling of the architecture will be explored, with potential applications in compact RF front-ends, and on-chip electromagnetic systems.

Towards Quantitative Comparisons of Bulk and Local Optoelectronic Properties of Emerging Solar Cell Materials with Interdigital Electrodes

CNF Project Number: 86300
Principal Investigator(s): John A. Marohn
User(s): Azriel Finsterer

Affiliation(s): Cornell University Chemistry and Chemical Biology

Primary Source(s) of Research Funding: NSF Award DMR-2113994gy

Contact: john.marohn@cornell.edu

Primary CNF Tools Used: Hamatech Hot Piranha Cleaner, Class II Resist Spinners, Edge Bead Removal System, ABM Contact Aligner, Hamatech Wafer Processor, Oxford Plasma Etchers (81 and 82), SC4500 Odd-Hour Evaporator, SC4500 Even-Hour Evaporator, Disco Dicing Saw

Abstract:

Gold interdigitated electrodes with varying electrode length and separation have been fabricated using a simple photolithography procedure. Fabricated electrodes were used in space charge-limited current experiments with a thin film of N,N'-Bis(3-methylphenyl)-N,N'-diphenylbenzidine embedded in a polystyrene matrix. Future work aims to combine such experiments with scanned-probe microscopy experiments to quantitatively compare bulk and local optoelectronic properties.

Summary of Research:

Gold interdigitated electrodes have been fabricated with a simple photolithography procedure, shown in Figure 1. Four-inch, standard-thickness quartz wafers were purchased from Mark Optics and were cleaned using the Hamatech hot piranha cleaner. Cleaned wafers were dehydrated at 180□ for 10 minutes and introduced to the spin coater, where they were coated with LOR resist. LOR was dispensed dynamically at 400 rpm for 4 seconds before coating at 4000 rpm for 45 seconds. The layer was soft-baked for 20 minutes at a wafer temperature of

180□ before S1805 resist was deposited statically with a coating speed of 4000 rpm for 60 seconds with an acceleration of 1000rpm/s. The film was soft-baked at 115□ for 3 minutes. The edge bead was removed with the edge bead removal system.

Figure 2 depicts the exposure array used to determine the optimum dose for wafer patterning. An octagonal mask with an opening was placed between the light source and the wafer on the ABM contact aligner. The experiment tested 8 distinct exposure conditions, varying the exposure time from 1 second to 4.5 seconds in 0.5-second increments. The wafer was developed with 726 metal ion-free developer sprayed in a single puddle for sixty seconds post-exposure. Optical microscopy revealed that 3.5 seconds of exposure—corresponding to a dose of 41.7-53.6 mJ/cm2—was sufficient for producing the desired pattern and undercut.

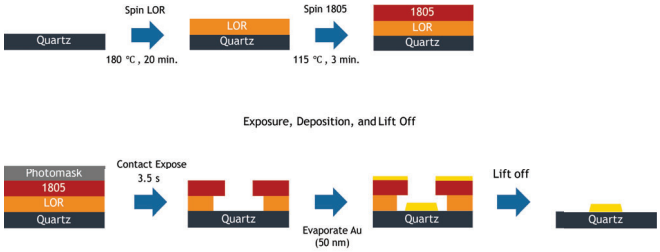

Figure 1: Schematic representation of the fabrication of gold interdigitated electrodes. Specific parameters are provided where possible.

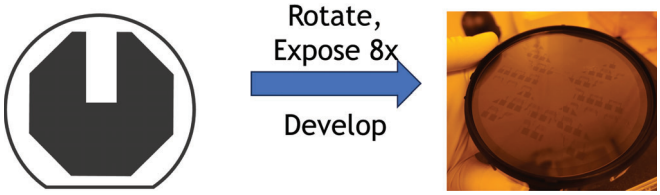

Figure 2: Schematic of the exposure array. Each region of the wafer was patterned using a distinct exposure dose. Determination of the ideal exposure dose was performed with optical microscopy.

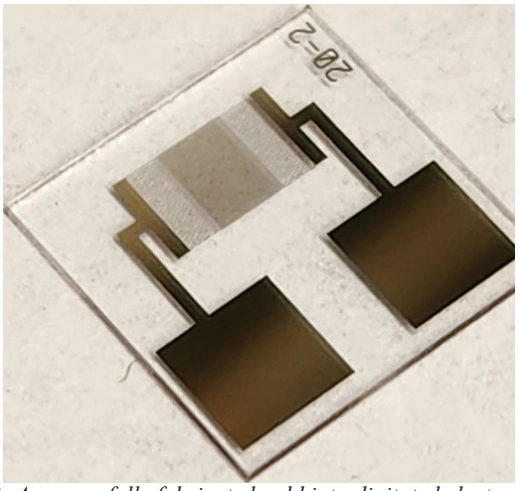

Figure 3: A successfully fabricated gold interdigitated electrode. The two numbers to the right of the electrode represent the separation of each digit in microns, while the second number signifies the length of each digit in millimeters.

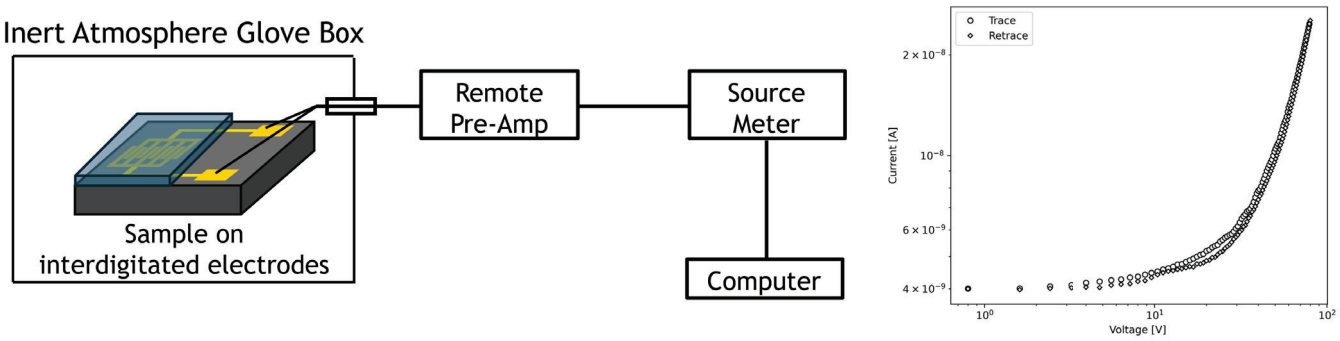

Figure 4: Block diagram of the space charge limited current experiment with a sample current voltage curve. The observed non-linearity in the current voltage curve is direct evidence of space charge-limited current injection.

Patterned wafers were placed in the Oxford 81 plasma etcher for a light oxygen plasma descum with a forward power of 50 mW for 45 seconds before being directly introduced into the Odd Hour Evaporator. When the bell jar pressure was ~ 2x10-6 Torr, 5 nm of chromium was deposited at a rate of ~1.4 Å/s, followed by the deposition of 50 nm of gold at a rate of 0.4 Å/s. The wafer was removed, and the metal was lifted off with Remover PG before being diced in the disco dicing saw. A representative electrode produced from the protocol is shown in Figure 3.

Electrodes were used in charge injection experiments involving the molecularly doped polymer system N,N'-Bis(3-methylphenyl)-N,N'-diphenylbenzidine in polystyrene. This system is known to produce space charge-limited current and provides a baseline for testing the electrodes1. A block diagram of the charge injection experiment and current-voltage curve is shown in Figure 4. The non-linearity of the current-voltage curve is direct evidence of space charge-limited current injection into the thin film. The bulk charge mobility of the film can be determined from the current-voltage data and can be subsequently compared to local mobility values determined with scanned-probe microscopy experiments[2].

Conclusions and Future Steps:

Gold interdigitated electrodes were fabricated using a simple photolithography procedure. These were implemented in space charge-limited current experiments involving a molecularly doped polymer, where space charge-limited current was directly observed as a non-linearity in the current-voltage curve. Using an established theory for space charge-limited current injection, the bulk charge mobility in the film can be determined.

Future work aims to incorporate the current-voltage curve experiment into a scanned probe microscopy experiment, where an oscillating cantilever charged with a frequency and amplitude modulated AC voltage will be brought over conductive thin films deposited on interdigitated electrodes operating in the space charge regime. Measuring the frequency shift as a function of the frequency modulation frequencies will yield a spectrum that can be used to quantitatively extract the charge density, charge mobility, and conductivity of the film. By modifying the amount of voltage applied to the electrode, measurements can be taken when the electrodes are operating under ohmic and space charge-limited current conditions, allowing for a robust test of the theory used to quantitatively extract key local optoelectronic properties.

References:

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