Circuit Integration and Chip Design

CNF Project Number: 325925
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Primary CNF Tools Used: Heidelberg MLA150 MasklessAligner, SC4500 Odd-Hour Evaporator, DISCO Dicing Saw and Westbond 7400A Ultrasonic Wire Bonder

Abstract:

This project focused on the design, fabrication, and testing of a compact circuit integrated into a packaged chip, optimized for impedance behavior analysis. The circuit, composed of capacitors, inductors, and resistors, was carefully designed and laid out for on-chip integration. The inductors were implemented using meander line structures, while the capacitors were realized as interdigitated fingers, together replicating the desired impedance characteristics. The fabricated chips are currently in the testing phase.

Summary of Research:

In this research, we developed a new circuit model consisting of capacitors, inductors, and resistors, which when configured as shown in Fig. 1a produce a desired impedance profile. The initial stage of the project involved theoretical analysis to extract the target circuit parameters, including the required capacitance, inductance, and resistance values. Subsequently, the focus shifted to translating these theoretical values into a practical layout by designing the individual passive components. Rather than designing the complete circuit in a single step, we adopted a modular approach: capacitors and inductors were designed separately and later integrated and optimized to match the desired impedance response. The layout designs were carried out using Keysight ADS, where we explored various geometries and material configurations. Specifically, capacitors and inductors were designed with different dimensions and using various metal layers, such as gold and aluminum, to achieve the same target values. Finally, the individual components were integrated into a complete layout, and the design was optimized to ensure that the overall impedance closely matched the theoretical predictions. The finalized designs were then exported as GDS files, ready for fabrication as seen in Fig. 1b.

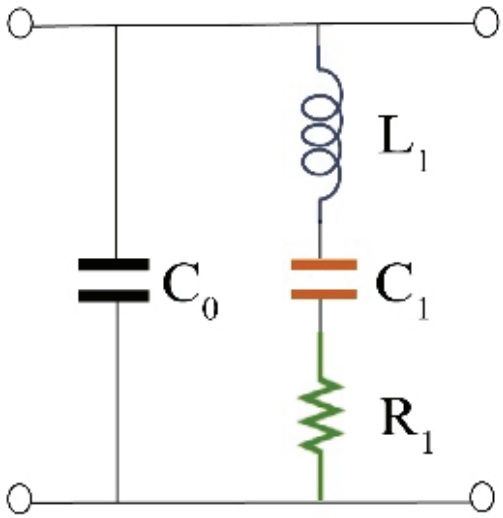

Figure 1a Topology of designed circuit.

At CNF, the fabrication process began with the selection of a 100 mm, prime-grade, n-type silicon wafer. Standard photolithography steps were followed, starting with spin-coating the wafer with a positive photoresist. Maskless lithography was then performed using the Heidelberg MLA 150 system, which enabled direct laser exposure of the desired pattern onto the photoresist without the use of a physical mask. Following exposure, the wafer was developed using an appropriate solvent, resulting in the transfer of the designed pattern onto the photoresist layer. After development, a metal deposition was carried out using the SC4500 Odd-Hour Evaporator. Two different metal stacks were deposited on separate wafers: one with a 1 μm-thick gold layer and the other with a 100 nm-thick aluminum layer. Upon completion of metal deposition, the wafers underwent a lift-off process (refer to Fig. 2a and 2b) to remove the remaining photoresist and define the final patterned metal structures. After the metal deposition and completion of the lift-off process, the wafer was diced into individual dies corresponding to the various unit cell designs developed during the initial design phase as seen in Fig. 3a. These discrete unit cell dies

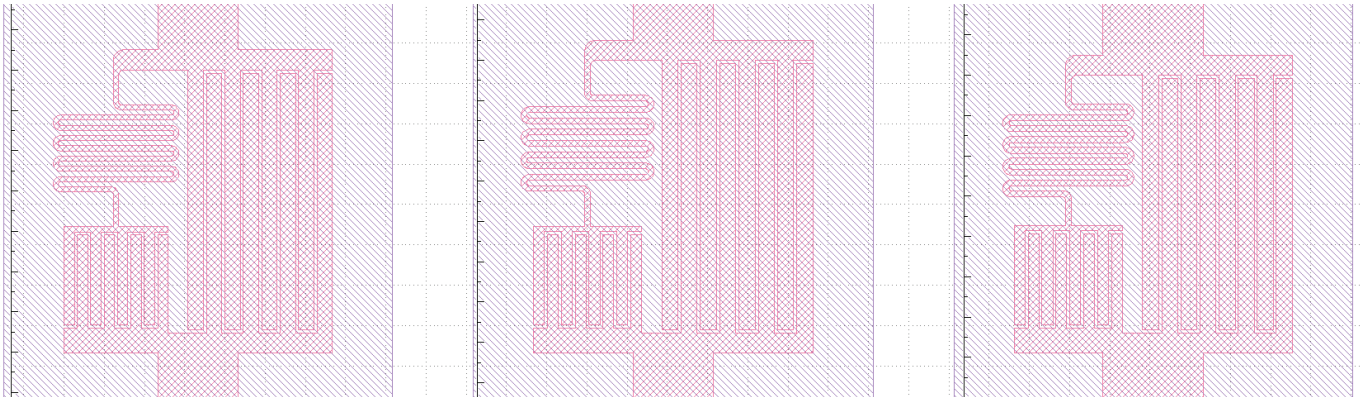

Figure 1b Layout of three different designs.

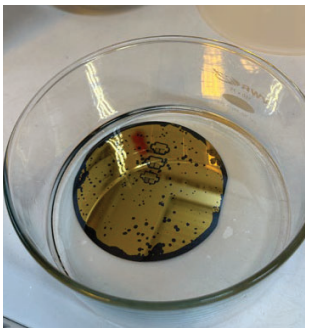

Figure 2a Lift-off process.

Figure 2b Wafer after Lift-off with designed metallic patterns.

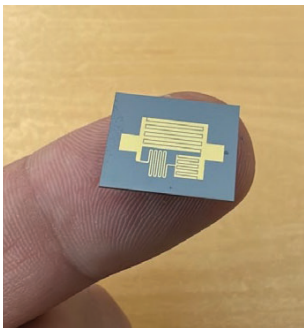

Figure 3a Diced unit cell.

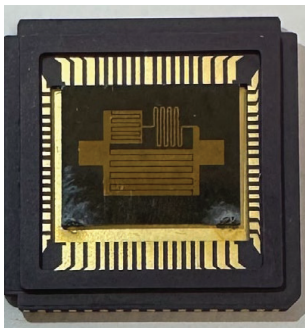

Figure 3b The fabricated circuit in a package.

were subsequently mounted and wire-bonded onto chip carriers for packaging shown in Fig. 3b. The packaged devices are currently in the final stages of preparation for preliminary measurements. We will characterize the fabricated devices by extracting key parameters such as S-parameters and impedance (Z) parameters, and compare the measured data against theoretical predictions. Based on any observed discrepancies, we will iteratively refine the initial designs and adjust intermediate fabrication steps to optimize performance. This cycle of design, fabrication, measurement, and analysis will be repeated until the desired device specifications are met.

Conclusions and Future Steps:

Based on the measurement results obtained, we will fine-tune specific design parameters to enhance alignment with theoretical predictions. Thus far, we have successfully designed and fabricated a single-order circuit unit cell. Moving forward, we plan to extend this work by developing and vertically stacking multiple unit cells to realize higher-order circuit architectures, which will also be fabricated on-chip. This work establishes a systematic design-to-fabrication workflow for custom impedance-engineered circuits at the microscale. The approach enables rapid prototyping and experimental validation of novel circuit topologies directly in integrated form. As the project progresses, further optimization and scaling of the architecture will be explored, with potential applications in compact RF front-ends, and on-chip electromagnetic systems.