Aluminum CMP Planarization for Graphene FETs

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Primary CNF Tools Used: Logitech Orbis CMP / Aluminum

Abstract:

As silicon CMOS technology approaches its scaling limits, graphene offers a compelling alternative due to its high carrier mobility, atomically thin profile, offering strong electrostatic control and promising high-frequency performance. However, roadblocks such as device-to-device variation, high contact resistance, poor dielectric interfaces, and non-uniform graphene quality have limited the adoption of graphene field - effect transistors (GFETs). In this work, we directly compare two GFET structures through a controlled, side-by-side process split to evaluate the impact of gate electrode topography (raised vs. recessed buried local gate) in terms of device performance and device-to-device variation. While the top performing devices remained similar across the three proposed structures, very significant differences are seen in terms of yield and device-to-device variation in the proposed variations. The device-to-device variation of the hole mobility dropped from 36% to 19%, device yield increased from 54.4% to 65.1%, Dirac voltage was reduced from 1.2 V to 0.7 V when a recessed local-back gate is used as opposed to a raised local-back gate. As such, this study shows that a direct comparison of process conditions can help identify favorable process conditions to improve the manufacturability of graphene-based transistors.

Summary of Research:

The integration of a planarization process for the fabrication of GFETs with hBN dielectrics, results in both a smoother transition from channel to gate as shown in schematically in Figure 1, and Figure 2. The planarization process provides a statistical improvement in the performance and variability of graphene transistors in terms of Dirac point and mobility when compared to a raised gate architecture as shown in Figure 3 and Figure 4. Hysteresis measurements (not shown) also indicate that the level of traps in the hBN/graphene interface is similar between the raised and recessed process. When compared to other dielectrics such as Al2O3 [1], hBN also offers advantages in terms of yield and contact resistance when used in a local-back gate process. In addition, the observed parameter variability is much reduced with the use of hBN as a dielectric due to better material compatibility during processing, which along with other process improvement and considerations, could lead to the needed improvement in yield and reliability [2], [3], [4]

Conclusions and Future Steps:

While prior studies have aimed to improve GFET performance or reduce variability, most work has typically done so in evaluating disparate device structures, materials, or fabrication flows, and focusing only on "hero" devices that do not reflect broader statistical trends. In contrast, our work systematically integrates monolayer hBN as a gate dielectric and a CMP-recessed aluminum gate within a unified fabrication platform, enabling direct, controlled comparisons across design variations. This approach not only enhances key performance metrics, such as contact resistance, mobility, and cutoff frequency, but also dramatically reduces device-to-device variation and increases yield. By analyzing full device distributions rather than peak values alone, this study offers critical insights into how dielectric choice and gate geometry together influence reproducibility. Demonstrating a substantial reduction in device variability, the standard deviation of extracted hole mobility decreased from 36% to 18%, while device yield improved significantly from 54.4% to 65.1%. The Dirac point shifted closer to 0 V (from ~1.2 V to 0.7 V), and the contact resistance was reduced from 0.75 kΩ to 0.67 kΩ. Ultimately, our findings establish practical design and process guidelines for realizing scalable, high-performance graphene electronics to bridge gaps between isolated breakthroughs and manufacturable, wafer-level technologies. The reduction in device-to-device variation indicates that a process induced variation may be mitigated through the presented work.

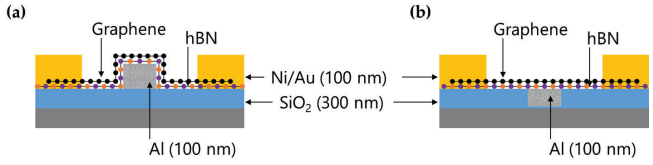

Figure 1: Device cross-section for (a) raised Al gate with hBN gate dielectric and (b) recessed Al gate with hBN gate dielectric.

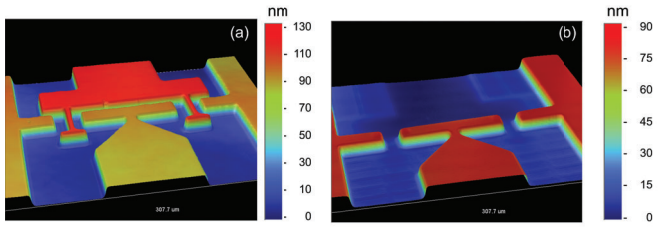

Figure 2: Three-dimensional white light interferometry scans of fabricated (a) raised and (b) recessed Al/hBN/graphene field effect transistors.

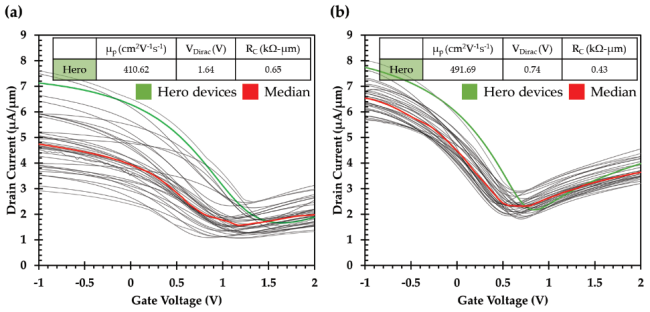

Figure 3: Transfer characteristics overlay at VDS = 0.1 V of fabricated graphene FETs with a gate length of 10 μm drain current normalized to its width of 20 μm and contact resistance (RC) normalized to its width (a) raised Al gate with monolayer hBN gate dielectric and (b) recessed Al gate with monolayer hBN gate dielectric.

The finding implies that extending the process flow to further large-scale integration may support a more uniform device array and a scalable, multi-user circuit design platform. By analyzing full device distributions rather than peak metrics alone, this study reveals how dielectric selection and gate geometry directly influence reproducibility. The observed consistency suggests that this hBN/ recessed gate structure is a strong candidate for an optimal platform of scalable, and high-performance GFET fabrication.

References:

[1] T. J. Huang, A. Ankolekar, A. Pacheco-Sanchez, and I. Puchades, "Investigating the Device Performance Variation of a Buried Locally Gated Al/Al2O3 Graphene Field-Effect Transistor Process," Applied Sciences (Switzerland), vol. 13, no. 12, Jun. 2023, doi: 10.3390/app13127201.

[2] S. Fukamachi et al., "Large-area synthesis and transfer of multilayer hexagonal boron nitride for enhanced graphene device arrays," Nature Electronics 2023 6:2, vol. 6, no. 2, pp. 126–136, Feb. 2023, doi: 10.1038/s41928-022-00911-x.

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[4] "IRDSTM 2023: Beyond CMOS and Emerging Materials Integration - IEEE IRDSTM." Accessed: Jul. 24, 2025. [Online]. Available: https://irds.ieee.org/editions/2023/20-roadmap-2023-edition/126-irds%E2%84%A2-2023-beyond-cmos-and-emerging-materials-integration

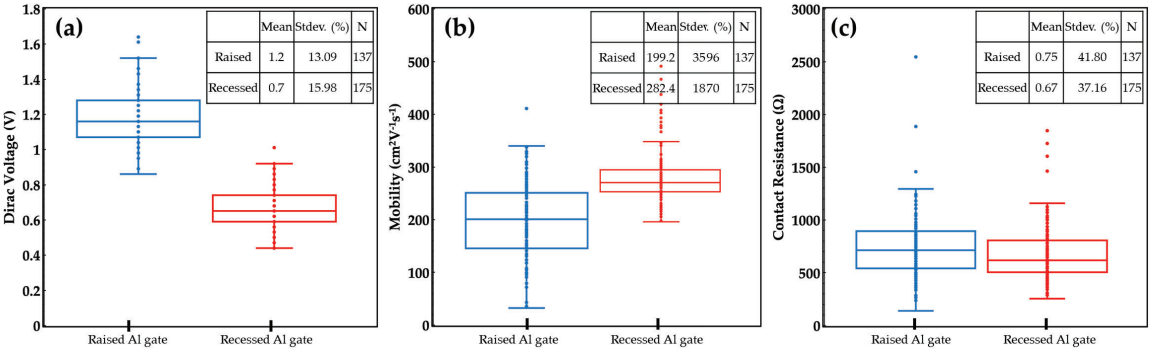

Figure 4: Box and whisker comparison of performance and variation of fabricated devices with raised and recessed aluminum gates in relation to (a) mobility, (b) Dirac voltage, and (c) contact resistance. Within each box and whisker plots, inset indicate the average, % standard deviation and number of working devices for each group.