SUPREME Tasks 6/7

CNF Project Number: 307823
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Primary Source(s) of Research Funding: SRC/DARPA

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Primary CNF Tools Used: ABM Contact Aligner, SUSS MA6-BA6 Contact Aligner, Unaxis 770 Deep Silicon Etcher, AJA Ion Mill, AJA Sputter Deposition, Veeco Savannah ALD, Electroplating Hood – Au/Cu, P7 Profilometer, Zygo Optical Profilometer,HFTL DC Probe Station, HFTL Small-Signal Probe Station

Abstract:

For heterogeneous integration of millimeter-wave transceiver frontends, we compare the millimeter-wave loss of coplanar interconnects fabricated on Si interposers with different resistivities. Coplanar interconnects 2146-μm long are laid out on two types of Si substrates: HR Si (resistivity > 1 kΩ·cm, thickness = 155 μm) and doped Si (resistivity < 10 Ω·cm, thickness = 205 μm). Small-signal measurements from 1 GHz to 40 GHz indicate the advantages of high-resistivity (HR) Si interposers for heterogeneous integration of millimeter-wave circuits.

Summary of Research:

The width of the center electrode of the coplanar interconnect and its gap to the ground electrode are 30 μm and 16 μm, respectively, resulting in a characteristic impedance ≈ 50 Ω. The ground electrodes are grounded by a high density of through-silicon vias (TSVs) to suppress higher-order modes. To mitigate the residual stress from thermal expansion mismatch, TSVs are metallized with Al having an annular structure (Fig. 1) [1]. Front-side wafer fabrication comprises mainly sputtering of 20-nm Ti and 1.5-μm Al and patterning by liftoff. The most critical steps of backside fabrication involve etching and metallizing 50-μm-diameter TSVs. Using the Bosch process [2] with a 200-nm Al2O3 hard mask, the substrates are deep etched from the backside at an etch rate of 27 nm/s. TSV metallization is then carried out by depositing 50-nm Pt using atomic layer deposition [3], followed by 70-nm Ti and 2-μm Al using sputtering (Fig. 2) [4]. DC measurements confirm a TSV series resistance on the order of 1 Ω. Small-signal millimeter-wave on-wafer measurements (Fig. 3) show the coplanar interconnect fabricated on HR Si have an insertion loss of 0.7 dB/mm at 40 GHz (Fig. 4), an order of magnitude better than the same coplanar interconnect fabricated on doped Si. The return loss of the coplanar interconnect fabricated on HR Si is always greater than 20 dB between 1 and 40 GHz.

Conclusions and Future Steps:

The above result confirms that it is necessary to use HR Si (as opposed to doped Si) as an interposer for heterogeneous integration of millimeter-wave transceiver frontend. In the future, HR Si of different resistivities will be compared to determine the optimum resistivity level.

References:

[1] M. Leskela and M. Ritala, Thin Solid Films 409, 138 (2002).

[2] F. Laermer et al., IEEE Microelectromech. Syst. 211 (1999).

[3] X. Sun et al., IEEE Electron Packag. Technol. 76 (2011).

[4] S. M. Rossnagel, IBM J. Res. Dev. 43, 163 (1999).

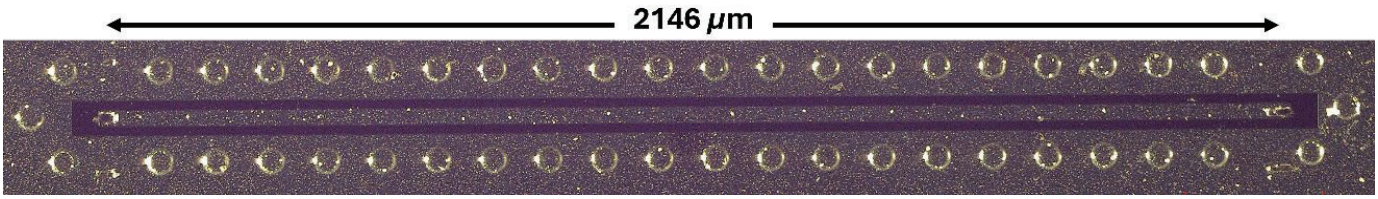


Fig. 1. Micrograph showing a 2146-μm-long grounded coplanar interconnect within two parallel rows of TSVs to prevent higher-order modes from propagating.

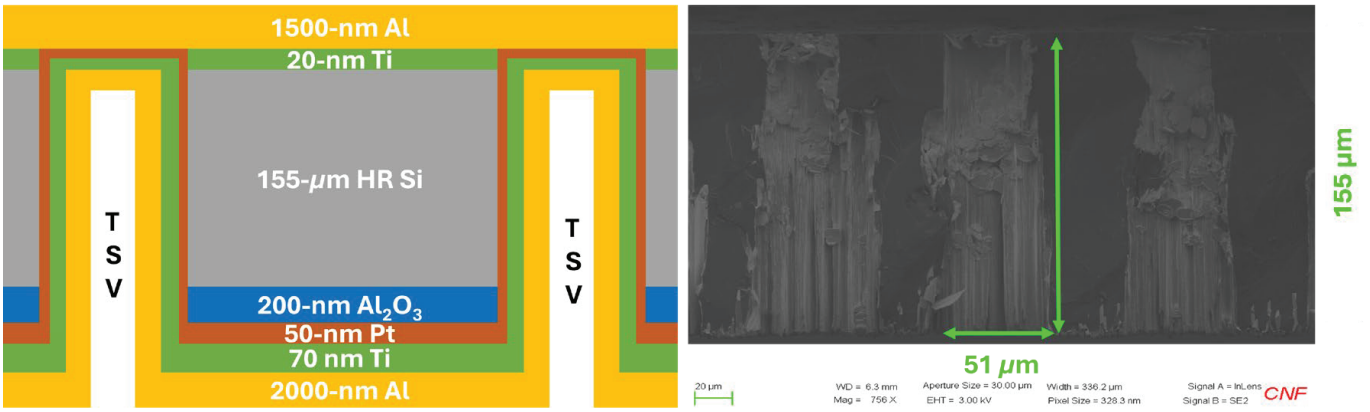


Fig. 2. Cross-section (a) schematic and (b) SEM image of a metallized through-Si via (TSV).

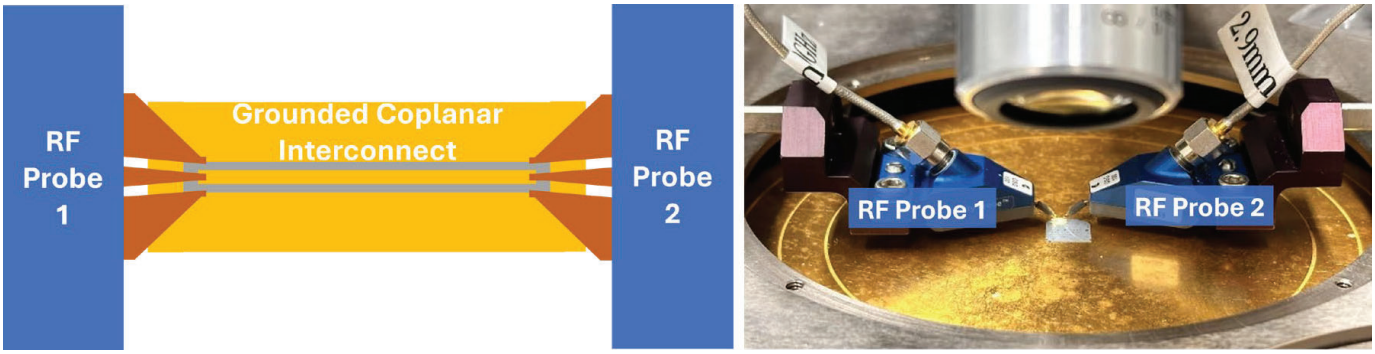
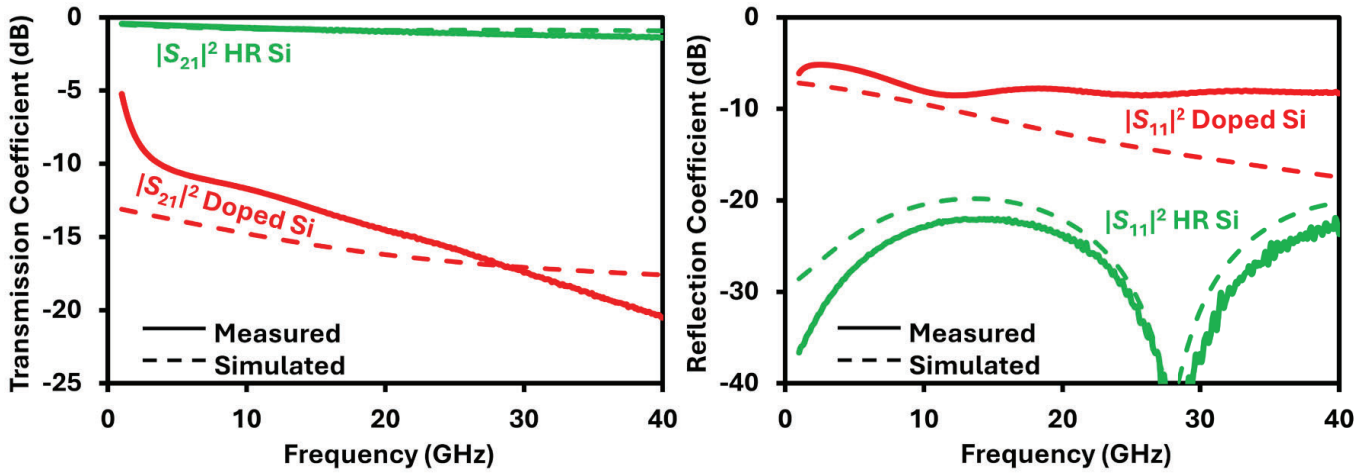


Fig. 3. (a) Schematic and (b) photograph of coplanar interconnect under millimeter-wave test.



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