Cornell NanoScale Facility High School Summer Internship

CNF Project Number: CNF Summer Internship
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Primary CNF Tools Used: Oxford 81, Oxford 82, ASML DUV Stepper, P7 Profilometer, Zeiss Supra SEM, Unaxis 770 Deep Silicon Etcher, Plasma-Therm Versaline Deep Silicon Etcher, Oxford Cobra ICP Etcher, Gamma Automatic Coat-Develop Tool

Abstract:

Our internship was mainly spent between two projects: characterization of multiple different tools and cleanroom upkeep, maintenance, and development. We helped to install new gas lines for compressed air and house nitrogen in an upstairs lab space. We also assisted in orbital welding a new exhaust pipe to a cleanroom etcher. Our other main project was working towards characterizing many different etch recipes on multiple Reactive Ion Etching (RIE) tools. We ran various etches, measuring the feature step-heights after pre-etch, etch, and cleaning processes. Late in our data-collection, we realized our measurements were incorrect when we calculated negative process selectivity rates. We attribute this error to noise in our larger measurements registering as larger than the change in photoresist height, potentially caused by multiple issues in our process. While we are disappointed by this, we have learned much about the levels of exactitude required in the cleanroom as well as how to consider acceptable margins of error and stay within them.

Summary of Research:

Our characterization project focused on running etch recipes on multiple tools throughout the lab and measuring pre-, during-, and post-process step-heights. We could then take that data, calculate etch rates and selectivity, and compare it to previously collected data to determine how each tool functioned now versus in the past. This could illuminate tool issues or determine needed recipe adjustments as tools age.

Our characterization happened in several waves. In the first, we grew silicon nitride, silicon oxide, and polysilicon layers on silicon wafers before spinning photoresist and exposing and developing our pattern.

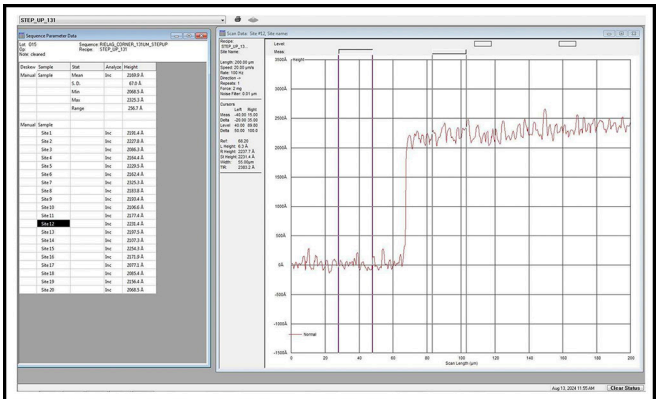

Figure 1: Noisy P7 Profilometer Data on an Oxide Wafer.

Figure 2: Compressed Air (left) and House Nitrogen Gas Lines Ran in Lab 238. We installed six of these valves and their pipework under Paul's supervision.

We then performed an anti-reflective coating (ARC) etch on each wafer before using the P7 Profilometer to measure the step-height of our pattern's features. We utilized a measurement sequence that took step-height measurements at 20 different locations across the wafer's surface to characterize the selectivity of each tool. Afterwards, we ran various etch recipes on the wafers using both the Oxford 81 and 82 (Table 1). After using the P7 to measure the post-etch height, we conducted a photoresist clean on the wafers before performing a final post-process measurement on each wafer.

In the second wave, we performed a similar process with bare silicon wafers using the Unaxis 770 Deep Silicon Etcher, the Oxford Cobra ICP Etcher, and the Plasma-Therm Versaline Deep Silicon Etcher (Table 2). Our process was identical to the first wave, beginning with an ARC etch, moving to the characterization etch, and ending with a photoresist clean, though this wave, we ran recipe duplicates. We used the same sequence on the P7 to measure each wafer after ARC etch, characterization etch, and clean. Unfortunately, we eventually determined that much of our data was unusable towards characterization due to noise in our measurements appearing larger than the change in photoresist height (Figure 1). This resulted in a negative selectivity rate.

We also decided to duplicate the processes done on the Oxford 81 and 82 in a third wave of wafers. This would not only fill in some data gaps from the first wave, but also provide us with a second set of data points to verify our findings. This third wave data, however, also proved to be critically mismeasured, again containing measurement noise that obscured the change in photoresist height. Many small issues with our measurements could have caused the overlarge noise, including problems in our sample loading, unseen profilometer needle slant, and a lack of clear parameters for acceptable data results, causing overlarge margins of error. We are disappointed by these nonresults; yet we have learned much through our mistakes. We have gained key knowledge on how to avoid small inaccuracies and mismeasurements that can sum into critical issues by clearly defining acceptable error margins and catching errors as they appear.

Additionally, we assisted Paul Pelletier, Senior Process Engineer, in many different tasks around the cleanroom, its service chassis, and other CNF lab spaces. We began working with him as he introduced us to the basics of high-purity gas line welding and cutting. We helped him weld and install a new exhaust line with a removable section for the Oxford 100 ICP Dielectric Etcher. Upcoming research in the CNF cleanroom will involve analyzing chemical compounds found in etching tool exhausts, making a removable exhaust necessary. Paul also gave us an introduction in working with copper and stainless-steel piping when we installed compressed air and house nitrogen lines above the ceiling in a second-floor lab space (Figure 2). We learned to fit, bend, and cut these pipes as well as how to analyze a space and think creatively around problems.

Recipe Name	RF Power (Watts)	CF4 Flow Rate (sccm)	CHF3 Flow Rate (sccm)	SF6 Flow Rate (sccm)	Ar Flow Rate (sccm)	O2 Flow Rate (sccm)	Oxide Wafers Run	Nitride Wafers Run	Polyoxide Wafers Run
CF4	150	30					1	1	1
CHF3+Ar	200		45		15		1		
CHF3+O2 Oxide	150/200		50			2	1		
CHF3+O2 Nitride	150		50			5		1	
Si anISO 100 mm	100		26	26		17			1

Table 1: Oxford 81 and 82 Recipes and Wafers Ran. Note that the CHF3+O2 Oxide recipe ran at 150 watts on the Oxford 82, while the 81 ran at 200.

Tool	Unaxis	Unaxis	Versaline	Cobra
Process	0trench	Photonics	IAT	HBr+Ar PR 2
Time/Loops	80 loops	5 mins	100 loops	10 mins

Table 2: Etch Recipes Ran on Each Deep Silicon Etcher.

Conclusions and Future Steps:

Our time as interns at CNF has been a great learning experience and engaging job for both of us. Working at a well-established facility with such experienced and knowledgeable staff is an opportunity that most don't get, much less directly after high school. Though the summer was short, we learned many different skills, from tool-operation and handling to report-writing and professional interaction. We also learned much about handling mistakes and unexpected outcomes, developing our response and correction skills. On a broader scale, CNF was both our first in-depth introductions to microelectronics and nanoscale work. We walk away from this internship with increased knowledge of what it means to work in the nanoscale field and the many opportunities it holds, information that may impact our futures as we head into our first year of college and beyond.

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