Through-Silicon Vias for Substrate-Integrated Waveguides

CNF Project Number: 3078-23
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Primary Source(s) of Research Funding: SUPREME Center funded by SRC/DARPA

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Primary CNF Tools Used: ABM Contact Aligner, SUSS MA6-BA6 Contact Aligner, AJA Sputter Deposition – 1 & 3, UNAXIS 770 Deep Silicon Etcher, AJA Ion Mill, Zygo Optical Profilometer

Abstract:

As the demand for heterogeneous-integrated RF chips emerges, substrate-integrated waveguides (SIWs) based on through-silicon vias (TSVs) have become increasing important due to their low loss and high power capacity across a wide frequency range. In particular, above 110 GHz, SIWs are small enough to be integrated in Si interposers for high-power interconnects. They can also be used to form high-quality passive devices such as filters and antennas, which have been difficult to integrate on chip. This enables system on chip. In this study, we investigate the fabrication of SIWs in Si interposers with a thickness on the order of 100 um. The thin Si wafers were patterned and etched using the Bosch deep reactive ion etching (DRIE) process to create TSVs. Preliminary results indicate an etch rate of approximately 27 nm/s, which is too slow to etch through the Si interposer. Work is in progress to improve the etch rate.

Summary of Research:

Silicon (Si) is most extensively used material in semiconductor devices due to its exceptional electrical and mechanical properties, including a high dielectric constant, electrical resistivity, breakdown strength and low loss tangent. These characteristics make it an attractive candidate for SIWs. However, its relatively low mechanical toughness and high thermal conductivity compared to materials like silicon carbide (SiC) pose challenges during processing, particularly in etching processes. Our group has successfully demonstrated SiC as a viable substrate material for SIW processing. The methodology developed for SiC SIW fabrication is adapted as a proof of principle for Si SIW fabrication.

To demonstrate the feasibility and develop a processing recipe for Si SIWs, we obtained a thinned high-resistivity Si wafer with a thickness of approximately 150 μm and resistivity of > 1000 ohm-cm. Drawing from a similar approach used for SiC SIWs, our methodology began with depositing a 50 nm layer of aluminum oxide (Al_2O_3) on the frontside of the Si wafer as an etch stop layer. This deposition was carried out using AJA Sputter Deposition – 1, achieving a deposition rate of approximately 2.8 Å/s.

Following this, the frontside was patterned using an ABM Contact Aligner, after which a titanium/aluminum (Ti/Al) layer was deposited using AJA Sputter Deposition – 2 to metalize the frontside. Concurrently, the backside of the wafer was patterned, and Al_2O_3 was deposited to define the etching pattern for TSVs. Al_2O_3 is chosen for its excellent masking properties in the Bosch DRIE process for Si, offering a selectivity as high as 1:1000.

For the DRIE, UNAXIS 770 Deep Silicon Etcher was used. To facilitate effective cooling during the reactive etching, the Si wafer was bonded to a sapphire carrier wafer using cool grease. The etching chemistry used was C_4F_8/SF_6, which reacts with and removes Si to create the vias anisotropically.

Using a Zygo Optical Profilometer, we repeatedly measured the depth of the TSVs and observed an etch rate of 3.3 Å/loop or approximately 27.3 nm/s throughout the process as shown in Figure 1.

Due to the fragility of the thinned Si wafer, precautions were taken during post-etching processes when removing cool grease and carrier wafer. Dicing streets were drawn on the Si wafer as shown in Figure 2, to facilitate simultaneous etching for easier detachment and dicing into smaller chips. Finally, the etch stop layer was physically removed using an AJA Ion Mill, and the backside was metallized with Ti/Al using AJA Sputter Deposition – 2 to fill the TSVs and establish connections to the frontside. The Si wafer after etching is shown

Figure 1: Zygo Optical Profilometer image for TSV depth measurement.

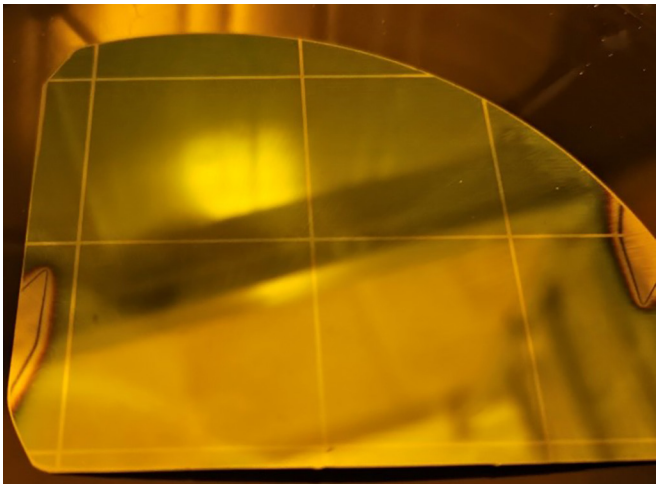

Figure 2: Dicing street pattern on Si wafer.

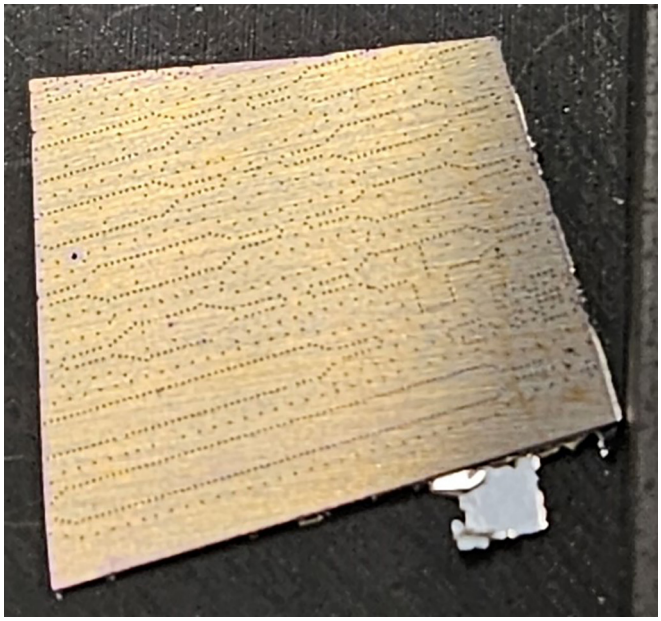

Figure 3: Si SIW chip after the Bosch DRIE process.

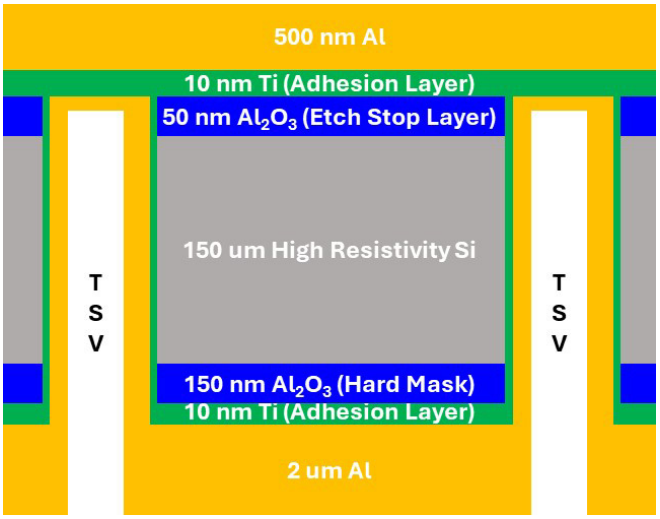

Figure 4: Structure of Si SIW.

in Figure 3 and the structural details and final product configurations are illustrated in Figure 4, showcasing the possibility of processing SIWs with thinned high resistivity Si wafers.

Conclusion and Future Steps:

The fabrication of Si SIWs focused on studying the Bosch DRIE of thinned Si wafers, achieving an etch rate of 27 nm/s with uniform anisotropic etching across the wafer. With the etching process proven feasible, the next phase involves investigating the most effective methods and materials for metallizing the SIWs, particularly to fill the TSVs. Initially, atomic layer deposition (ALD) of platinum (Pt) is planned to coat the chip. Pt is chosen for its superior properties in enhancing interconnect reliability compared to Ti, which is prone to oxidation, potentially compromising device quality. Following the completion of processing steps, measurements will be conducted at the High Frequency Test Lab (HFTL) using the 220 GHz single-sweep probe station located at Cornell University. This comprehensive testing environment will provide critical insights into the performance and functionality of the fabricated SIWs at high frequencies.

References:

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