Lithography for Topological Nanowires

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Primary CNF Tools Used: JEOL 6300, PT 720 etcher, CVC SC4500 Combination Thermal/ E-gun Evap System, Zeiss Supra SEM, Nabity Nanometer PGS, YES Asher, Woollam RC2 Spectroscopic Ellipsometer

Abstract:

The resistivity scaling of copper interconnects with decreasing dimensions remains a major challenge in the continued downscaling of integrated circuits, which causes increased signal delay and power consumption in the circuits [1]. Therefore, new materials are needed for the next generation of interconnects beyond the 7 nm technology node. Topological semimetals like molybdenum phosphide (MoP), owing to their topologically protected surface states and suppressed electron backscattering, show promising resistivity values compared to copper interconnects at nanometer scale [2]. Here, with the assist of electron beam lithography and reaction ion etching, we successfully synthesized 1D topological MoP nanowires with tunable line width and thickness to investigate its resistivity scaling effect at nanometer scale.

Summary of Research:

The fabrication flow chart of single crystalline topological MoP is shown in Figure 1. We start from commercially available single crystalline molybdenum disulfide (MoS_2) bulk crystals. Single crystalline MoS_2 flakes exfoliated from bulk crystals were placed on dry thermal oxide silicon wafer. These wafers were pre-patterned with alignment girds designed by our lab to locate flakes of interest (Figure 2a). First round of e-beam exposure was performed using JEOL 6300 to produce the dumbbell-shaped pattern as the mask of etching. Then, reactive ion etching was performed using PT720 etcher with SF_6 etchant to etch away MoS_2 in the exposed area, leaving the dumbbell-shaped MoS_2 with 1D wire in the middle (Figure 2b). SF_6 fluorinates top layers of PMMA, making them hard to remove by acetone. Therefore, O_2 plasma etching using the same tool was subsequently performed to remove the top layer of fluorinated PMMA. Then, using template-assisted chemical vapor deposition (CVD), the MoS_2 nanowire was converted to 1D MoP nanowire by reacting with PH_3 gas (Figure 2c). To deposit electrodes and measure the resistance, second round of e-beam lithography was done using Nabity-NPGS system to produce the electrode pattern. After descum in YES Asher, 10 nm chromium and 100 nm gold was deposited on the wafer as electrodes using SC4500 evaporator. After lift-off, the device was done and ready for measurement.

Figure 3 (a) shows the scanning electron microscope (SEM) images of the 1D topological MoP nanowire synthesized via the method described above with a line width of 80 nm (left) and 30 nm (right), separately. Figure 3 (b) shows the Raman spectra of the wires before and after conversion. Before conversion, the E12g and A1g peaks of MoS_2 can be clearly seen at 384 and 409 cm-1, respectively. After conversion, the two Raman modes of MoS_2 disappeared and one peak at about 402 cm-1 shows up, which is an indication of MoP according to the literature [3]. Wires with any other designated line width can be fabricated by changing the pattern arrangement, e-beam dose, or the etching time. Wires with different thickness can also be fabricated through choosing exfoliated MoS_2 flakes of different thicknesses. This method thus provides an excellent approach for fabricating 1D topological nanowires to investigate the unconventional resistivity scaling effect expected for them.

References:

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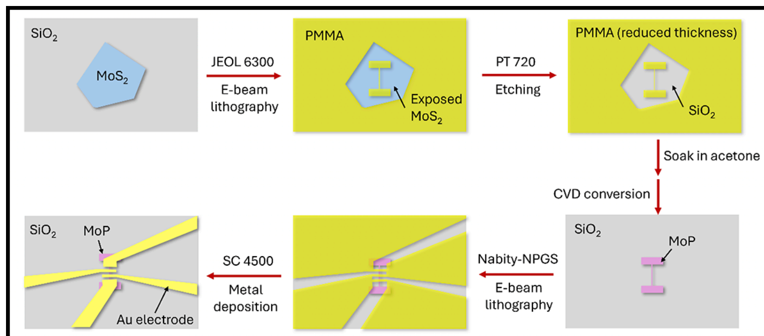

Figure 1: Process flow of 1D MoP nanowires as well as the 4-point transport measurement devices.

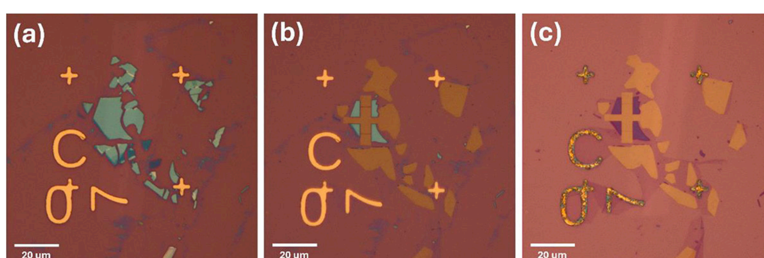

Figure 2: (a) Exfoliated MoS_2 on the pre-patterned dry thermal oxide wafer. (b) Dumbbell shaped MoS_2 with 1D nanowires in the middle after e-beam lithography and etching. (c) 1D MoP nanowires after template-assisted CVD conversion from MoS_2.

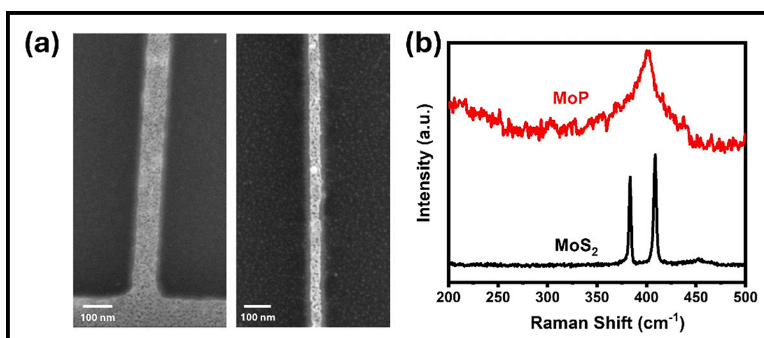

Figure 3: (a) SEM images of 1D topological MoP wires with line width of 30 nm (left) and 80 nm (right). (b) Raman spectra of MoS_2 and converted MoP wires.

PROCESS & CHARACTERIZATION