Atomic Layer Deposition of High-K Dielectrics

CNF Summer Student: Sarah Levine
Student Affiliation: Civil Engineering, Worcester Polytechnic Institute

Summer Program(s): 2024 Xing Army Educational Outreach Program (AEOP), 2024 Cornell NanoScale Facility Research Experience for Undergraduates (CNF REU) Program

Principal Investigator(s): Professor Grace (Huili) Xing, Electrical and Computer Engineering, Cornell University

Mentor(s): Jeremy Clark, Cornell NanoScale Science and Technology Facility, Cornell University

Primary Source(s) of Research Funding: 2024 Xing Army Educational Outreach Program (AEOP), National Science Foundation under Grant No. NNCI-2025233

Contact: sjlevine@wpi.edu, grace.xing@cornell.edu, clark@cnf.conrell.edu

Summer Program Website: https://cnf.cornell.edu/education/reu/2024

Primary CNF Tools Used: Arradiance ALD Gemstar-6, AJA Sputter -2, SC4500 Odd-Hour Evaporator, Woollam RC2 Spectroscopic Ellipsometer, Hamatech Hot Piranha, Oxford 81/82 Etcher, Everbeing EB-6 Probe Station with Keithley SMU, Rapid Thermal Anneal -AG Associates Model 610

Abstract:

To keep making the world's most powerful central processing units faster and more energy-efficient dielectrics are used to increase the capacitance of these devices. Conventional HfO2-based high K dielectrics gate stacks cannot produce such a small effective oxide thickness and the consequent high capacitance without removing the interfacial SiO2, which negatively impacts electron transport and gate leakage current. The superlattice gate stacks offer much-reduced leakage current and zero mobility deterioration as they lack the need for this kind of scavenging. The gate stacks are used in GaN transistors for power and communication, the existing dielectric in these transistors causes significant leakage and damages the underlying material. Ultrathin ferroic HfO2-ZrO2 multilayers, stabilized with competing ferroelectric–antiferroelectric order, offer a new method for advanced gate oxide stacks in electronic devices beyond traditional HfO2-based high-dielectric-constant materials. The project aims to develop a process to deposit the high-K HfO2/ZrO2superlattices whose new layers will help lower charge leakage. Atomic Layer Deposition (ALD) is used to build up the superlattice, we use ALD because it provides uniform and precisely tuned thickness, then through various depositing methods such as sputtering and e-beam evaporation aluminum was deposited through a capacitor shadow mask and then annealed through rapid thermal processing. The fabricated devices were characterized on a DC probe station and graphed for Capacitance -Voltage (C-V), to solve for the dielectric constant, also known as K, and also examine other material parameters such as defect density. The project works towards the smallest leakage at the smallest equivalent oxide thickness.

Summary of Research:

In capacitors, a tried and tested industry dielectric is SiO2, which has a dielectric constant of 3.9. HfO2 has become a forefront dielectric in the past few years with a dielectric constant between 18 and 25. The issue with this is that the smaller you make these capacitors, the higher the chance for electron leakage. The proposed HfO2/ZrO2 superlattice has new added layers that should help prevent such leakage and allow for a higher dielectric constant to be obtained. The goal is to be able to achieve smaller equivalent oxide thicknesses and keep leakage down.

The main part of this research has been to develop a process flow to deposit these high K dielectric HfO2/ZrO2superlattice devices. The first step in this process was to perform a hot piranha etch to get rid of any lingering organic material on the N-type silicon substrate. Next was to deposit the superlattice on the silicon substrate through Atomic Layer Deposition, which allowed for layer-by-layer deposition with increased control over thickness and composition at a relatively low growth temperature, which for this superlattice was 200°C. To determine the amount of loops used for each precursor ellipsometry was done to determine how much deposition was laid down with 300 loops. It was determined that 11 loops of ZrO2 would be about equivalent to 1.2 nm whereas 3 loops of HfO2 is about equivalent to 0.4 nm.

The next step in the process was to deposit aluminum and metalize the capacitor. This was done either through sputtering or e-beam evaporation. The sputtering while giving an incredibly uniform coating emits x-rays as a consequence of using plasma which can damage the sample. The evaporator was unable to provide that

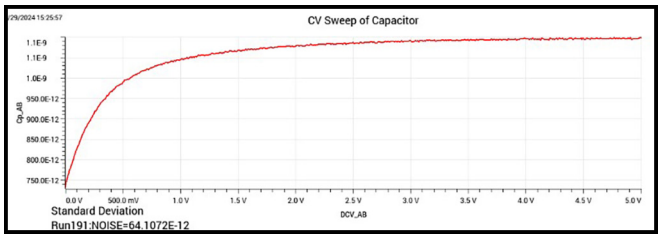

Figure 1: A CV sweep of a HfO2capacitor of voltage over capacitance in farads.

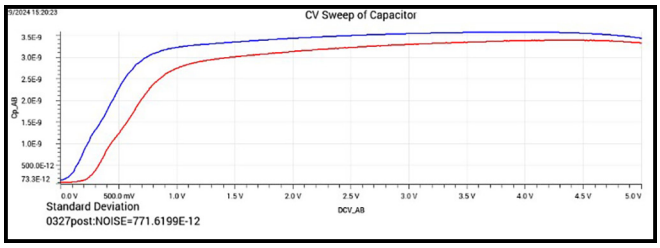

Figure 2: A CV Sweep of the capacitor of voltage over capacitance in farads. These graphs were used to determine the K dielectric of the capacitor. This particular sweep is of the Period x4 made on the evaporator, the red line is the pre-annealed data and the blue is the post-annealed.

same guaranteed uniformity, but aluminum has such a relatively low evaporation rate that the silicon substrate isn't as harmed by any x-rays emitted from e-beam evaporation. When depositing the superlattice residual deposition also ends up on the back side of the wafer, to remove this reactive ion etching, specifically a CF4 etch, is used. To protect the capacitors, a clean silicon wafer was placed over the capacitors to not allow any CF4 to etch off the needed dielectric. Aluminum is then deposited onto the back to improve overall contact resistance and thermal conduction.

The final step in the fabrication process is to perform rapid thermal annealing (RTA) using N2 at 200°C for one minute. Characterization of these capacitors was done on a DC probe station and a Capacitance-Voltage (C-V) test was conducted. To test the C-V sweep and confirm our equation,

$$C = \frac{k\epsilon_0 A}{d}$$

solving for k, a sweep with HfO2 as the dielectric was done resulting in pre-annealed data of 17.7. The graph for this data is shown in Figure 1, which is on the lower end of the expected dielectric constant range which confirmed the test being done.

Conclusions and Future Steps:

The data collected from the Capacitance-Voltage graphs, shown in Figure 3, showed the expected decrease in the dielectric constant as film thickness also decreased.

Period, Aluminum Deposition Method	Pre-Annealing Dielectric Constant	Post Annealing Dielectric Constant
x 1, Sputter	1.65	2.63
x 1, Evaporator	1.34	2.25
x 2, Sputter	1.13	2.83
x 2, Evaporator	3.37	3.25
x 4, Sputter	7.03	8.61
x 4, Evaporator	7.16	7.56
x 8, Sputter	11.30	11.12
x 8, Evaporator	11.27	9.66
x 12, Sputter	15.08	14.74
x 12, Evaporator	12.19	12.57

Figure 3, above: A chart of the different periods of pre-annealed and post-annealed dielectric constants. Figure 4, below: A picture of one of the wafers Levine fabricated through sputtering.

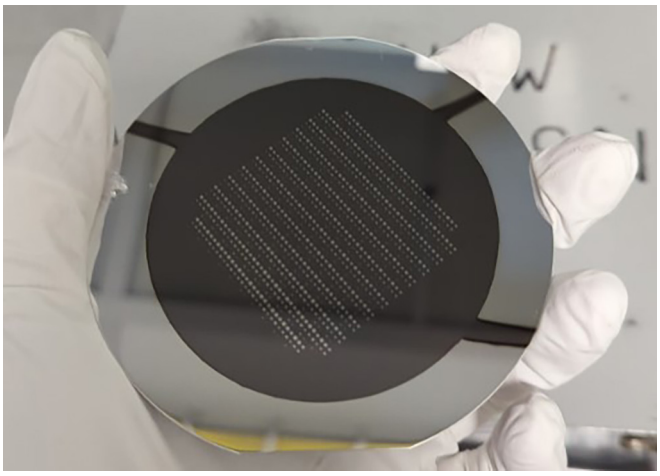

Figure 2 shows what a graph of pre and post-annealed date would look like for this C-V sweep. In the post-anneal data, it showed an increase in the dielectric constant for the thinner films after being annealed.

Future work on this project will be to take the superlattice and confirm the thicknesses through X-ray reflectivity (XRR) measurements and that will also ensure the ALD recipe is producing the film growth at the expected rate. Another step that could be taken to ensure the best dielectric constant is to etch the native oxide layer. Looking at higher annealing temperatures would be another variable that could increase the dielectric constant. Measuring the capacitors on different graphs such as doing a SMU-Sweep to characterize current versus voltage for leakage measurements.

Acknowledgements:

I would like to express my appreciation to my Principal Investigator Professor Grace (Huili) Xing, the Jena-Xing Group, and my mentor Jeremy Clark. This project would have been unsuccessful without their guidance. This work was performed at the CNF, an NNCI member supported by NSF Grant NNCI-2025233.