Fabrication and Characterization of High-Resistivity Silicon Interposers

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Primary CNF Tools Used: ABM Contact Aligner, SÜSS Contact Aligner, AJA Sputter 1 and 2, AJA Ion Mill, Unaxis 770 Deep Si Etcher, Zeiss Ultra SEM, Zygo Optical Profilometer, Glen 1000 Resist Strip, Veeco Savannah ALD, DC Probe Station, Microwave Small-Signal Probe Station

Abstract:

A recent focus of advancement in semiconductor technology involves the heterogeneous integration of chiplets on an interposer. Typically, the interposer is made of polymers, glass, or doped silicon. This work explores high-resistivity (HR, . > 1 kΩ·cm) silicon interposers fabricated at the Cornell NanoScale Facility for millimeter-wave applications. The most critical process is the etching and metallization of through-silicon vias (TSVs). The cross-sectional geometry of a TSV is shown in Figure 1. Using aluminum oxide (Al2O3) as a backside hard mask and a frontside layer of titanium as an etch stop layer, 155 μm deep silicon etching was successfully carried out with the Unaxis 770 Deep Silicon Etcher using the SF6/C4F8 Bosch Process. Subsequently, using an argon beam operating at 600 V and 295 mA with a vacuum of 10-8 torr, the frontside titanium layer was ion milled with a removal rate of 27 nm/s for 50 μm diameter TSVs. The TSVs were then metalized with a layer of platinum deposited using atomic layer deposition and sputtered titanium and aluminum, resulting in a series resistance of 2.5 Ω. The TSVs were also patterned for RF characterization to form grounded coplanar waveguides (GCPWs). The GCPWs were probed up to 40 GHz, resulting in an insertion loss of 2 dB/mm and a return loss of 26 dB at 40 GHz.

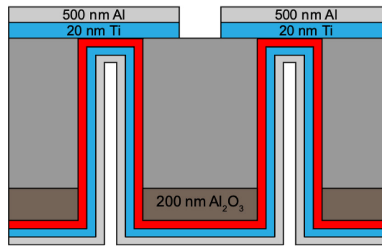

Figure 1: Cross-sectional geometry of through-silicon vias.

Summary of Research:

The fabrication process began by adapting a previously verified method for creating substrate integrated waveguides (SIWs) on silicon carbide and applying it to a doped silicon substrate. This process flow involved distinct frontside and backside processes: the frontside process produced structures necessary for interconnects, such as microstrip and coplanar transmission lines, while the backside process formed the geometry of the TSVs. The electrical testing results obtained from this initial set of samples were quite poor, with TSVs exhibiting non-ohmic characteristics. It was hypothesized that this issue stemmed from inadequate etching through the frontside aluminum oxide or inadequate metallization of the TSVs. For future samples, the fabrication process was adjusted by varying the incident angle and duration of the ion milling process, as well as the thickness of the platinum seeding layer for TSV metallization by atomic layer deposition (ALD). These adjustments resulted in an ohmic IV curve but with a significantly high TSV resistance of 14 ohms. Etching through the frontside aluminum oxide hard mask layer proved time-consuming and inconsistent, leading to the decision to remove the layer entirely with future samples. Testing on these subsequent samples showed that Bosch etching through the silicon substrate and ion milling through the frontside titanium layer yielded better TSV resistance and uniformity. These samples were analyzed using the Microwave Small-Signal Probe Station at frequencies up to 40 GHz. A 10 dB/mm insertion loss was observed with a 2146 μm grounded coplanar waveguide (GCPW), with consistent results across various samples and GCPW lengths. After the electrical characterization,

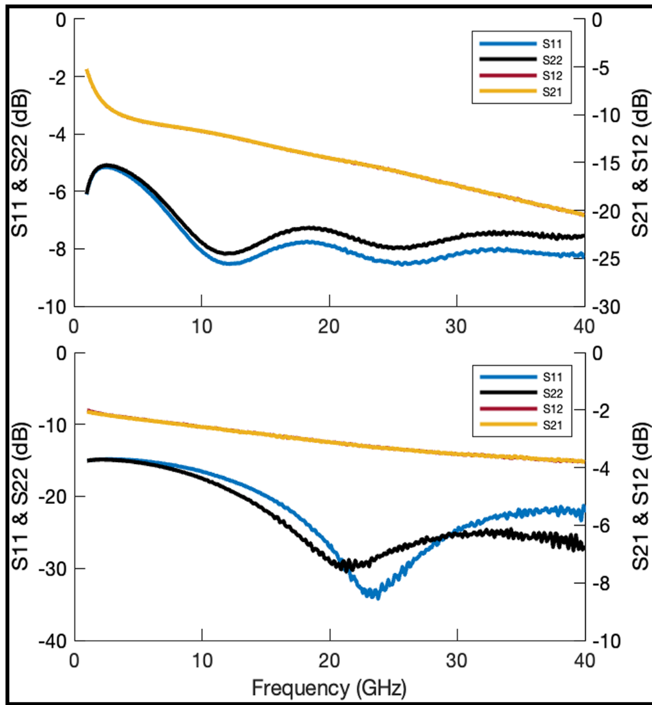

Figure 2: S-Parameters of 2146 µm GCPW test structures for doped silicon (above) and high-resistivity Si (below) up to 40 GHz.

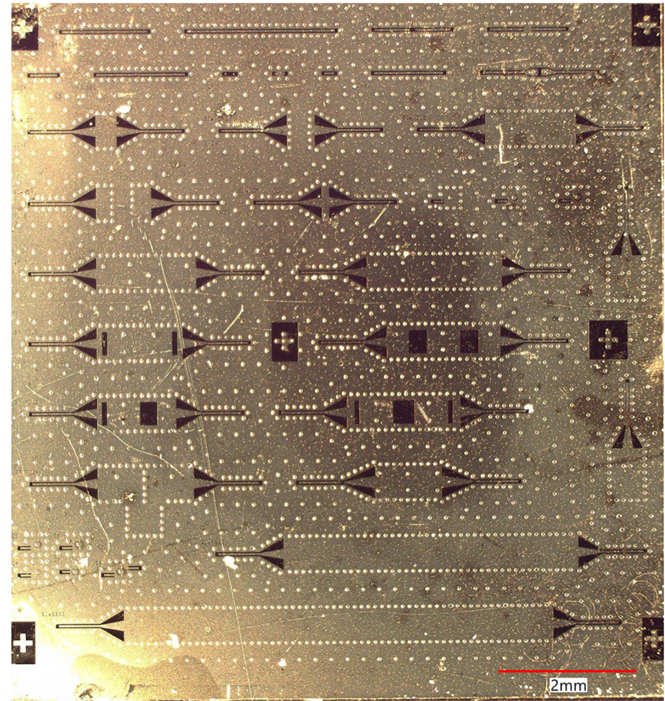

Figure 3: High-resistivity silicon sample, displaying frontside interconnect structures and backside TSVs.

the samples were cleaved to capture cross-sectional scanning electron microscope (SEM) images. The TSV dimensions observed in the SEM images were consistent with optical profilometer images taken earlier in the fabrication process and confirmed the successful sputtering of aluminum. This finalized procedure was then transferred from a doped silicon substrate to a high-resistivity silicon substrate. Electrical characterization of this sample yielded a TSV resistance of 2.5 ohms, with subsequent measurements using a 2146 μm GCPW indicating an insertion loss of 2 dB/mm and a return loss of 26 dB.

Conclusions and Future Steps:

A complete process flow for the fabrication of high-quality TSVs for use on doped silicon and high-resistivity silicon interposers has been developed and verified. However, a TSV resistance of less than 1 ohm remains to be achieved for a high-resistivity silicon sample. Moreover, the insertion loss of the fabricated high-resistivity silicon GCPWs is too high, making them unsuitable for effective use within their intended frequency range, the D-band (110-170 GHz). It is theorized that this is due to an insufficient amount of frontside aluminum, which was sputtered at a thinner thickness than anticipated.

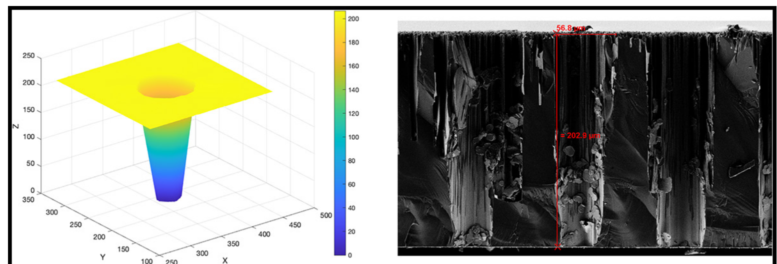
Figure 4: Optical profilometry image of TSV after through-substrate etching (left) and cross-sectional SEM image of TSV (right).

Acknowledgments:

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