# Fabrication of Superconducting Resonators on hBN Thin Films


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*Summer Program(s): 2024 Cornell NanoScale Facility Research Experience for Undergraduates (CNF REU) Program*

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*Primary CNF Tools Used: AJA Sputter 1 and 2, ABM Contact Aligner, Plasma-Therm 770 Etcher*



## Abstract:

Studying loss in superconducting devices is essential for high coherence quantum devices. Dielectric loss at the metal-substrate interface is a significant contributor to overall loss [1], which is why methods to study this important factor have been developed [2,3]. Hexagonal boron nitride (hBN) is a 2D material with several applicable properties, including low dielectric loss, chemical stability, and atomically flat surfaces free of dangling bonds, properties that make it an attractive material for integration into superconducting circuits [4]. In this research we employed a coplanar waveguide resonator design that is sensitive to dielectric loss at the metal substrate interface, comparing a "control" niobium (Nb)-on-sapphire resonator and an Nb-on-hBN-on-sapphire resonator.


## Summary of Research:

Superconducting resonators are used to characterize materials loss in superconducting quantum computers [5]. The chip design used in this research implements eight multiplexed quarter wave resonators inductively coupled to a feedline with tapered bond pads as shown in Figure 1a. Areas where metal is removed are shown in orange, and metallized areas are shown in white. This design allows for 1:1 comparisons of dielectric losses at the metal substrate interface [2].

Any given resonator, as visible in Figure 1c, exhibited a gap width g of 3 $\mu$m and conductor width s of 6 $\mu$m. This was also true for the feedline, and we qualified the resolution of our device features throughout our process development based on these metrics.

The original design, shown in Figure 1a, supports a 7.5 x 7.5 mm device size, and we were fabricating on 10 x 10 mm sapphire substrates. Upon completion of our devices, they would be brought to a controlled facility which supports a 6x6mm chip testing platform. We shrunk the design and added a guideline box around the device for improved mask alignment, better centering the new 6x6 mm device design (Figure 1b).

All 10 x 10 mm chips were cleaned via sonication for 10 minutes each in acetone, IPA, and water.

**Molecular Beam Epitaxy (MBE).** The first step in our device fabrication process was the growth of high-quality BN thin films via MBE on our ~ 500 $\mu$m thick sapphire substrate. Figure 2(a) shows resonant high-energy electron diffraction pattern indicating epitaxial quality of hBN film, Figure 2(b) is a Raman spectra showing the sharp characteristic hBN peak, and Figure 2(c) displays an AFM map of the film surface.

**Sputter Deposition.** After verifying the quality of our 5 nm thick hBN film, 600 Å of Nb were sputtered at the default 400 Watts on an AJA Sputter Deposition tool. In Figure 3, on the left side column, TEM of the hBN -Nb interface is shown to be damaged by the high-power metal ion bombardment.

We found, as shown in Figure 3 on the right-side column, that a lower sputter power of 50 watts maintained a pristine hBN film surface. Using a P7 profilometer, we determined that a sputter time of 10 minutes at this lower power yielded a 161Å thick layer of Nb. Therefore, a sputter time of 37.27 minutes or 2236.03 seconds would yield our desired 600Å of metal.

We were also interested in later comparing aluminum (Al) on sapphire and Al on hBN on sapphire resonators, so we also sputtered Al at 50 W for 10 minutes. Again, we used profilometry to determine an experimental

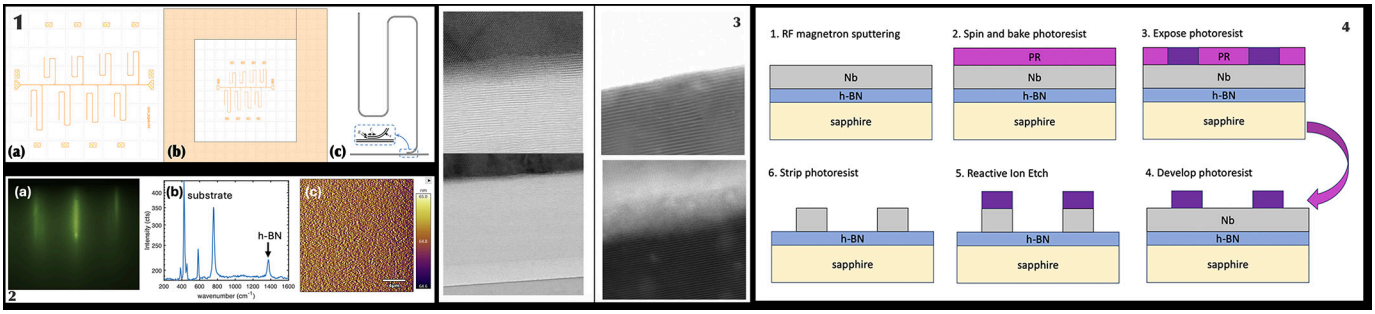


*Figure 1: Device mask design. (a) Original 7.5 x 7.5 mm design. (b) Modified 6 x 6 mm design with border for alignment. (c) A single superconducting resonator with gap width g and conductor width s. Diagram from Kopas, et al. [2]. Figure 2: (a) Electron diffraction pattern, (b) Raman spectra, and (c) AFM map of hBN thin film. Figure 3: TEM of Nb sputter at 400W (left) and 50W (right) on hBN thin film. Figure 4: Complete fabrication process.*

average of 265Å of sputtered Al through the 10-minute period.

**Photolithography.** We sputtered 60 nm Nb onto several 10 x 10 mm sapphire substrates in order to test and establish our photolithography process.

S1805 photoresist spun at 4000 rpm for 60 seconds yielded an average thickness of 500 nm. Our several resist-coated substrates were subsequently exposed at varying doses on the ABM Contact Aligner to determine the exposure time for optimal feature definition. The best exposure time was found to be 1.6 seconds.

**Reactive Ion Etch (RIE).** It was predicted that the RIE Cl2 etch chemistry on the Plasma-Therm 770 etcher could also affect the hBN thin film upon etching through the Nb. Thus, the first step to mitigate this issue was to accurately determine the Nb etch rate. After 36.7 seconds of etching our device pattern, we found that 36.8 nm of Niobium was etched and 36.57 nm of resist was etched. These measurements establish a 1:1 etch selectivity and 1nm/second etch rate.

A similar process was performed on the hBN where a pattern was etched for 15 seconds. We determined that the hBN thin film experienced an etch rate of ~ 1 nm/3 seconds after performing atomic force microscopy on a sample.

## Conclusions and Future Steps:

After establishing our etch process parameters, we would similarly verify the niobium was etched through by using a probe station to measure resistance between the gaps and the conductor, determining whether there is Nb in the gaps.

It has been shown that the superconducting transition temperature Tc of a metal can be affected by the substrate material [6]. We will observe this change using a Physical Property Measurement System, examining the change in resistance with varying extremely low temperatures.

As the pieces are required to conform to a 6 x 6 mm testing platform, they will be sent to DISCO laser dicing services.

Finally, the completed devices will be wirebonded and tested in a facility equipped with a He dilution fridge.

## Acknowledgements:

I would like to thank Cornell University, NNCI, and the NSF for funding this research via grant NNCI-2025233. Thank you to Joyce, Professor Zhiting Tian, and the staff at the Cornell NanoScale Facility for all the guidance and support throughout this project.

## References:

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[5] C. McRae, H. Wang, J. Gao, M. R. Vissers, T. Brecht, A. Dunsworth, D. P. Pappas, and J. Mutus. Review of Scientific Instruments 91, 091101 (2020).

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# Fabrication and Characterization of High-Resistivity Silicon Interposers


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*Primary CNF Tools Used: ABM Contact Aligner, SÜSS Contact Aligner, AJA Sputter 1 and 2, AJA Ion Mill, Unaxis 770 Deep Si Etcher, Zeiss Ultra SEM, Zygo Optical Profilometer, Glen 1000 Resist Strip, Veeco Savannah ALD, DC Probe Station, Microwave Small-Signal Probe Station*


## Abstract:

A recent focus of advancement in semiconductor technology involves the heterogeneous integration of chiplets on an interposer. Typically, the interposer is made of polymers, glass, or doped silicon. This work explores high-resistivity (HR, . > 1 kΩ·cm) silicon interposers fabricated at the Cornell NanoScale Facility for millimeter-wave applications. The most critical process is the etching and metallization of through-silicon vias (TSVs). The cross-sectional geometry of a TSV is shown in Figure 1. Using aluminum oxide (Al2O3) as a backside hard mask and a frontside layer of titanium as an etch stop layer, 155 $\mu$m deep silicon etching was successfully carried out with the Unaxis 770 Deep Silicon Etcher using the SF6/C4F8 Bosch Process. Subsequently, using an argon beam operating at 600 V and 295 mA with a vacuum of 10-8 torr, the frontside titanium layer was ion milled with a removal rate of 27 nm/s for 50 $\mu$m diameter TSVs. The TSVs were then metalized with a layer of platinum deposited using atomic layer deposition and sputtered titanium and aluminum, resulting in a series resistance of 2.5 Ω. The TSVs were also patterned for RF characterization to form grounded coplanar waveguides (GCPWs). The GCPWs were probed up to 40 GHz, resulting in an insertion loss of 2 dB/mm and a return loss of 26 dB at 40 GHz.


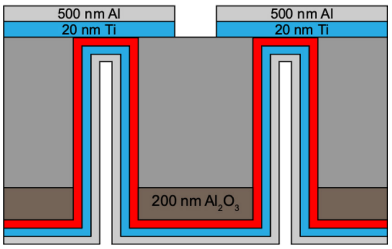


*Figure 1: Cross-sectional geometry of through-silicon vias.*

## Summary of Research:

The fabrication process began by adapting a previously verified method for creating substrate integrated waveguides (SIWs) on silicon carbide and applying it to a doped silicon substrate. This process flow involved distinct frontside and backside processes: the frontside process produced structures necessary for interconnects, such as microstrip and coplanar transmission lines, while the backside process formed the geometry of the TSVs. The electrical testing results obtained from this initial set of samples were quite poor, with TSVs exhibiting non-ohmic characteristics. It was hypothesized that this issue stemmed from inadequate etching through the frontside aluminum oxide or inadequate metallization of the TSVs. For future samples, the fabrication process was adjusted by varying the incident angle and duration of the ion milling process, as well as the thickness of the platinum seeding layer for TSV metallization by atomic layer deposition (ALD). These adjustments resulted in an ohmic IV curve but with a significantly high TSV resistance of 14 ohms. Etching through the frontside aluminum oxide hard mask layer proved time-consuming and inconsistent, leading to the decision to remove the layer entirely with future samples. Testing on these subsequent samples showed that Bosch etching through the silicon substrate and ion milling through the frontside titanium layer yielded better TSV resistance and uniformity. These samples were analyzed using the Microwave Small-Signal Probe Station at frequencies up to 40 GHz. A 10 dB/mm insertion loss was observed with a 2146 $\mu$m grounded coplanar waveguide (GCPW), with consistent results across various samples and GCPW lengths. After the electrical characterization,

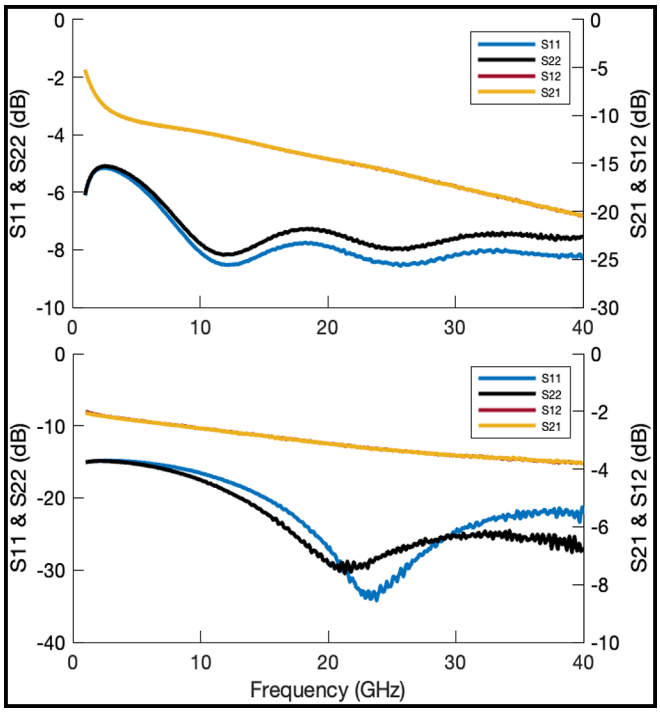


*Figure 2: S-Parameters of 2146 µm GCPW test structures for doped silicon (above) and high-resistivity Si (below) up to 40 GHz.*

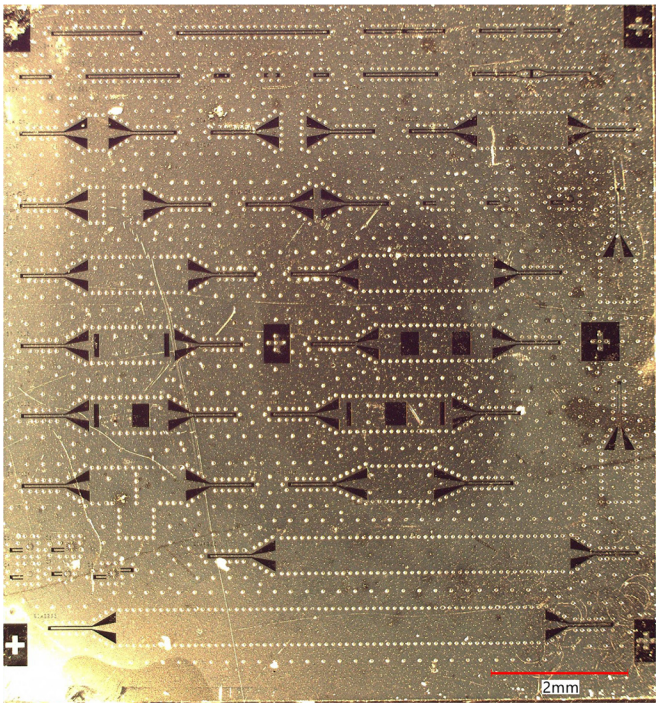


*Figure 3: High-resistivity silicon sample, displaying frontside interconnect structures and backside TSVs.*

the samples were cleaved to capture cross-sectional scanning electron microscope (SEM) images. The TSV dimensions observed in the SEM images were consistent with optical profilometer images taken earlier in the fabrication process and confirmed the successful sputtering of aluminum. This finalized procedure was then transferred from a doped silicon substrate to a high-resistivity silicon substrate. Electrical characterization of this sample yielded a TSV resistance of 2.5 ohms, with subsequent measurements using a 2146 $\mu$m GCPW indicating an insertion loss of 2 dB/mm and a return loss of 26 dB.

## Conclusions and Future Steps:

A complete process flow for the fabrication of high-quality TSVs for use on doped silicon and high-resistivity silicon interposers has been developed and verified. However, a TSV resistance of less than 1 ohm remains to be achieved for a high-resistivity silicon sample. Moreover, the insertion loss of the fabricated high-resistivity silicon GCPWs is too high, making them unsuitable for effective use within their intended frequency range, the D-band (110-170 GHz). It is theorized that this is due to an insufficient amount of frontside aluminum, which was sputtered at a thinner thickness than anticipated.

## Acknowledgments:

I would like to acknowledge the National Science Foundation (NSF) grant no. NNCI-2025233, the National Nanotechnology Coordinated Infrastructure (NNCI), and the Cornell NanoScale Facility for funding and curating the Research Experiences for Undergraduates (CNF REU) opportunity. Additionally, I would like to acknowledge and thank Yunjiang Ding, Xiaopeng Wang, and James Hwang for their invaluable guidance and support.

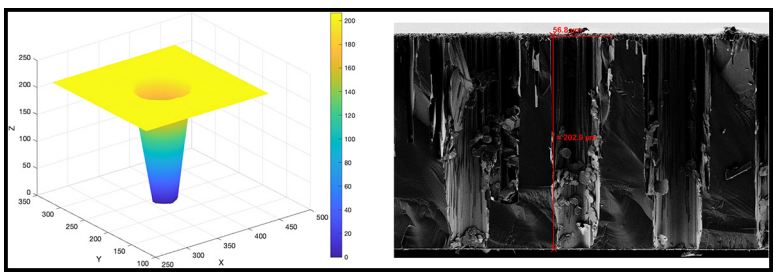

*Figure 4: Optical profilometry image of TSV after through-substrate etching (left) and cross-sectional SEM image of TSV (right).*

# Atomic Layer Deposition of High-K Dielectrics


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*Mentor(s): Jeremy Clark, Cornell NanoScale Science and Technology Facility, Cornell University*

*Primary Source(s) of Research Funding: 2024 Xing Army Educational Outreach Program (AEOP), National Science Foundation under Grant No. NNCI-2025233*



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*Primary CNF Tools Used: Arradiance ALD Gemstar-6, AJA Sputter -2, SC4500 Odd-Hour Evaporator, Woollam RC2 Spectroscopic Ellipsometer, Hamatech Hot Piranha, Oxford 81/82 Etcher, Everbeing EB-6 Probe Station with Keithley SMU, Rapid Thermal Anneal -AG Associates Model 610*



## Abstract:

To keep making the world's most powerful central processing units faster and more energy-efficient dielectrics are used to increase the capacitance of these devices. Conventional HfO2-based high K dielectrics gate stacks cannot produce such a small effective oxide thickness and the consequent high capacitance without removing the interfacial SiO2, which negatively impacts electron transport and gate leakage current. The superlattice gate stacks offer much-reduced leakage current and zero mobility deterioration as they lack the need for this kind of scavenging. The gate stacks are used in GaN transistors for power and communication, the existing dielectric in these transistors causes significant leakage and damages the underlying material. Ultrathin ferroic HfO2-ZrO2 multilayers, stabilized with competing ferroelectric–antiferroelectric order, offer a new method for advanced gate oxide stacks in electronic devices beyond traditional HfO2-based high-dielectric-constant materials. The project aims to develop a process to deposit the high-K HfO2/ZrO2superlattices whose new layers will help lower charge leakage. Atomic Layer Deposition (ALD) is used to build up the superlattice, we use ALD because it provides uniform and precisely tuned thickness, then through various depositing methods such as sputtering and e-beam evaporation aluminum was deposited through a capacitor shadow mask and then annealed through rapid thermal processing. The fabricated devices were characterized on a DC probe station and graphed for Capacitance -Voltage (C-V), to solve for the dielectric constant, also known as K, and also examine other material parameters such as defect density. The project works towards the smallest leakage at the smallest equivalent oxide thickness.


## Summary of Research:

In capacitors, a tried and tested industry dielectric is SiO2, which has a dielectric constant of 3.9. HfO2 has become a forefront dielectric in the past few years with a dielectric constant between 18 and 25. The issue with this is that the smaller you make these capacitors, the higher the chance for electron leakage. The proposed HfO2/ZrO2 superlattice has new added layers that should help prevent such leakage and allow for a higher dielectric constant to be obtained. The goal is to be able to achieve smaller equivalent oxide thicknesses and keep leakage down.

The main part of this research has been to develop a process flow to deposit these high K dielectric HfO2/ZrO2superlattice devices. The first step in this process was to perform a hot piranha etch to get rid of any lingering organic material on the N-type silicon substrate. Next was to deposit the superlattice on the silicon substrate through Atomic Layer Deposition, which allowed for layer-by-layer deposition with increased control over thickness and composition at a relatively low growth temperature, which for this superlattice was 200°C. To determine the amount of loops used for each precursor ellipsometry was done to determine how much deposition was laid down with 300 loops. It was determined that 11 loops of ZrO2 would be about equivalent to 1.2 nm whereas 3 loops of HfO2 is about equivalent to 0.4 nm.

The next step in the process was to deposit aluminum and metalize the capacitor. This was done either through sputtering or e-beam evaporation. The sputtering while giving an incredibly uniform coating emits x-rays as a consequence of using plasma which can damage the sample. The evaporator was unable to provide that

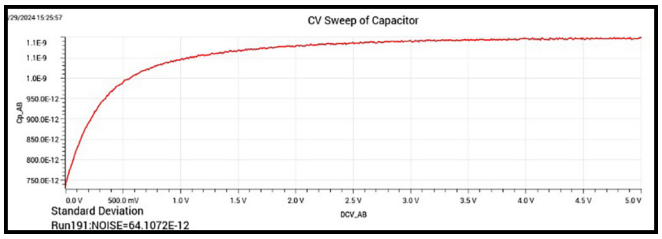


*Figure 1: A CV sweep of a HfO2capacitor of voltage over capacitance in farads.*

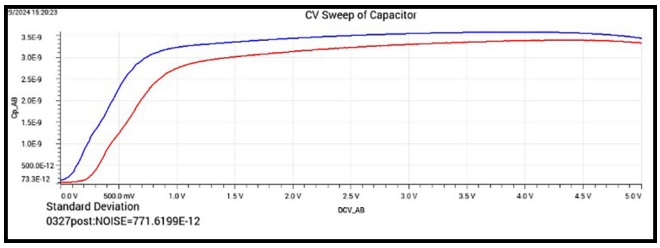


*Figure 2: A CV Sweep of the capacitor of voltage over capacitance in farads. These graphs were used to determine the K dielectric of the capacitor. This particular sweep is of the Period x4 made on the evaporator, the red line is the pre-annealed data and the blue is the post-annealed.*

same guaranteed uniformity, but aluminum has such a relatively low evaporation rate that the silicon substrate isn't as harmed by any x-rays emitted from e-beam evaporation. When depositing the superlattice residual deposition also ends up on the back side of the wafer, to remove this reactive ion etching, specifically a CF4 etch, is used. To protect the capacitors, a clean silicon wafer was placed over the capacitors to not allow any CF4 to etch off the needed dielectric. Aluminum is then deposited onto the back to improve overall contact resistance and thermal conduction.

The final step in the fabrication process is to perform rapid thermal annealing (RTA) using N2 at 200°C for one minute. Characterization of these capacitors was done on a DC probe station and a Capacitance-Voltage (C-V) test was conducted. To test the C-V sweep and confirm our equation,

$$C = \frac{k\epsilon_0 A}{d}$$

solving for k, a sweep with HfO2 as the dielectric was done resulting in pre-annealed data of 17.7. The graph for this data is shown in Figure 1, which is on the lower end of the expected dielectric constant range which confirmed the test being done.

## Conclusions and Future Steps:

The data collected from the Capacitance-Voltage graphs, shown in Figure 3, showed the expected decrease in the dielectric constant as film thickness also decreased.

| Period, Aluminum Deposition Method | Pre-Annealing Dielectric Constant | Post Annealing Dielectric Constant |
|---|---|---|
| x 1, Sputter | 1.65 | 2.63 |
| x 1, Evaporator | 1.34 | 2.25 |
| x 2, Sputter | 1.13 | 2.83 |
| x 2, Evaporator | 3.37 | 3.25 |
| x 4, Sputter | 7.03 | 8.61 |
| x 4, Evaporator | 7.16 | 7.56 |
| x 8, Sputter | 11.30 | 11.12 |
| x 8, Evaporator | 11.27 | 9.66 |
| x 12, Sputter | 15.08 | 14.74 |
| x 12, Evaporator | 12.19 | 12.57 |

*Figure 3, above: A chart of the different periods of pre-annealed and post-annealed dielectric constants. Figure 4, below: A picture of one of the wafers Levine fabricated through sputtering.*

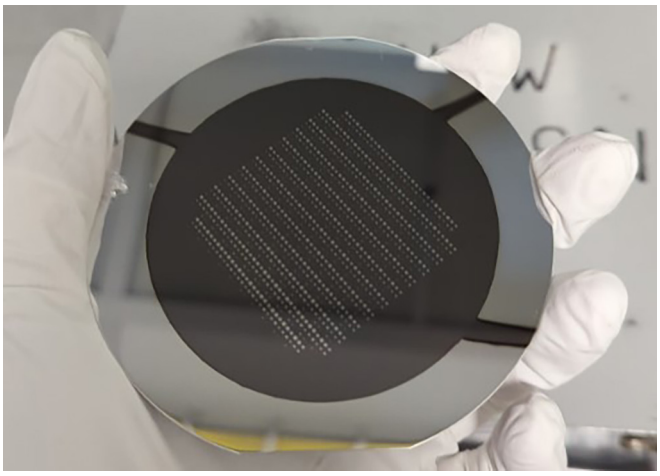

Figure 2 shows what a graph of pre and post-annealed date would look like for this C-V sweep. In the post-anneal data, it showed an increase in the dielectric constant for the thinner films after being annealed.

Future work on this project will be to take the superlattice and confirm the thicknesses through X-ray reflectivity (XRR) measurements and that will also ensure the ALD recipe is producing the film growth at the expected rate. Another step that could be taken to ensure the best dielectric constant is to etch the native oxide layer. Looking at higher annealing temperatures would be another variable that could increase the dielectric constant. Measuring the capacitors on different graphs such as doing a SMU-Sweep to characterize current versus voltage for leakage measurements.

## Acknowledgements:

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# Investigating the Lateral Spreading of Vanadium-Based Ohmic Contacts

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*2024 CNF REU Mentor(s): Joseph Dill, Department of AEP, Cornell University; Shivali Agrawal, Department of CBE, Cornell University; Xianzhi Wei, Department of MSE, Cornell University*

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*Primary CNF Tools Used: SC4500 Odd-Hour Evaporator, Zeiss Supra Scanning Electron Microscope (SEM), Bruker Quantax 200 Energy Dispersive X-Ray Spectroscopy (EDS), GCA AS200 i-line Stepper, Glen 1000 Resist Strip, RTA-AG610b*

## Abstract:

Aluminum Gallium Nitride (AlGaN) is a material of interest for the development of UV-emitting photonic devices. Vanadium-based metal stacks are a popular means of forming ohmic contacts to n-type AlGaN. However, these metal stacks must be annealed to temperatures above 600°C [6] for VN to form during which the metals in the ohmic contact stack can spread laterally and short patterned devices. The aim of this study is to determine the annealing conditions that minimize the lateral spreading of V/Al/Ni/Au stacks and investigate the behavior of these stacks under annealing. Metal stacks were patterned on 8 x 8 mm silicon (Si) pieces and annealed for different temperatures and times. A "safe zone" of annealing conditions that didn't short the devices was determined. The amount of spreading was determined from Scanning Electron Microscope (SEM) images of C-TLM structures. We also observed a "balling up" of the Ni under annealing, likely due to its high surface energy. This observation motivates switching Ni to a metal with a lower surface energy in future studies.

## Summary of Research:

**Background.** Since the first realization of the GaN blue LED in 1993 [1], research attention has been devoted to AlGaN-based light-emitting devices that would emit invisible UV light. Such devices would enable many novel technologies, including chemical-free sterilization of medical equipment and water purification [2]. One key challenge to this end is the formation of ohmic contacts to n-type AlGaN. Several studies have achieved low resistance contacts using annealed V/Al/X/Au metal stacks [6,7]. When annealed in $N_2$, V alloys with N to form VN on the surface, which has a work function of 3.55 [5]. The Al helps form donor-like N vacancies in the AlGaN, and Au prevents oxidation and provides a soft surface for electrical probing. X is the "diffusion barrier" metal, usually V or Ni. However, annealing these metal stacks often leads to strange and undesirable metallurgical effects, such as the formation of Ni domains [7].

**Methods.** Annealed metal pads were fabricated on 8 x 8 mm Si pieces as follows:.

1. Si pieces were cleaned in acetone, isopropyl alcohol (IPA), and deionized water for 5 minutes each with sonication to remove any organic contamination from the surface.
2. Pieces were spin-coated with AZ nLOF 2020 negative photoresist and baked.
3. Circular transmission line method (C-TLM) patterns were exposed using the GCA AS200 i-line Stepper, followed by a post-exposure bake.
4. The pattern was developed in 726 MIF developer for 30 sec.
5. An ozone descum was performed to remove all residual undeveloped photoresist.
6. A metal stack of 20nm of V, 80nm of Al, 40nm of Ni, and 100nm of Au was deposited by electron beam evaporation (see Figure 1).
7. Liftoff was performed by immersing the pieces in Microposit Remover 1165 and IPA with sonication.
8. Each sample was annealed in N2 ambient. The anneal times and temperatures for each sample are shown in Figure 2a.

**Results.** Figures 2b and 2c show SEM images of a C-TLM structure with 0.8.m spacing on samples 1 and

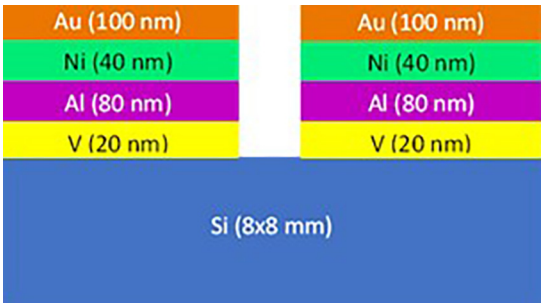


*Figure 1: Cross-sectional view of sample.*

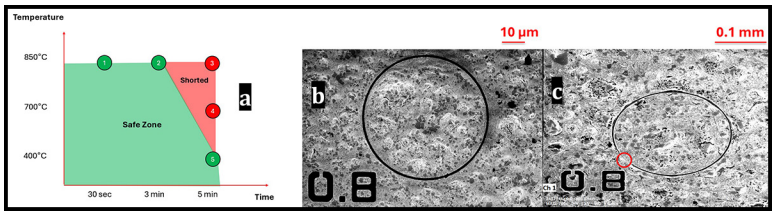


*Figure 2: Plot of each annealed sample with temperature vs time annealed in (a). Post-anneal SEM images in (b) sample 1: 850°C, 30 seconds and (c) sample 3: 850°C, 5 minutes. Red circle indicates shorting the in the C-TLM pattern.*

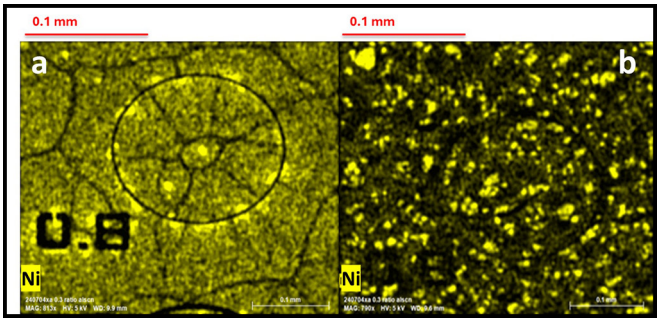


*Figure 3: EDS map of Ni in (a) sample 5: 400°C, 5 minutes and (b) sample 3: 850°C, 5 minutes.*

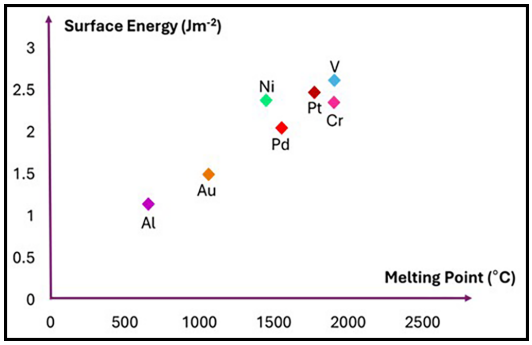


*Figure 4: Plot of surface energy vs melting point. Values obtained from [4].*

3, annealed at 850°C for 30 sec and 5 min, respectively. The red circle in 2c indicates a point where the C-TLM pad was shorted due to lateral spreading of the metal during annealing. The annealing conditions that did and didn't result in shorting of the 0.8.m pattern are summarized in Figure 2a. The annealing conditions for samples 1, 2, and 5 establish a "safe zone" in which annealing didn't cause shorting.

The annealed samples were imaged with Electron Dispersive X-Ray Spectroscopy (EDS) to investigate the motion of the constituent metals in the stack during annealing. As seen in Figure 3, Ni was observed to coalesce, forming domains that decreased in size with increasing anneal temperature. In sample 5, annealed at 400°C for 5 minutes, ~ 40 $\mu$m-wide domains formed (see Figure 3a), and in sample 3, annealed at 850°C for 5 minutes, ~ 5 $\mu$m-wide domains formed (see Figure 3b). This is likely a result of nickel's high surface energy.

## Conclusions and Future Steps:

During annealing, a metal can minimize its surface energy by forming a spherical shape rather than remaining flat. These spheres will be tighter at higher temperatures to minimize the additional thermal free energy. We observe the initial stages of this in Figure 3a wherein the Ni begins forming wide domains, presenting a "cracked" appearance. Ni's tendency to ball up during annealing is used by Shi et al. to form Ni nanoparticles annealing sputtered Ni thin films [3].

Considering these findings, future ohmic contact stacks should utilize a diffusion barrier with a lower surface energy than Ni. The surface energies and melting points of V, Al, Ni, Au, and alternate diffusion barrier metals (Pd, Pt, Cr) are benchmarked in Figure 4. Of the candidate metals, Pd has the lowest surface energy. Future studies should also be conducted on AlGaN, rather than Si, such that the electrical performance of the ohmic contacts can be investigated in parallel with the metallurgical behavior under annealing.

## Acknowledgements:

Special thanks to the Cornell NanoScale Science & Technology Facility Research Experience for Undergraduates (CNF REU) Program for hosting this internship. I would like to express my appreciation for the Jena-Xing Group, my PI Prof. Grace Xing, my mentors Joseph Dill, Xianzhi Wei, and Shivali Agrawal for their support and guidance.

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# Effect of Temperature on Particle Morphology Polymerized via Initiated Chemical Vapor Deposition in Liquid Crystal


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*Summer Program(s): 2024 Cornell Robert Frederick Smith School of Chemical and Biomolecular Engineering FMRG: Cyber (CBE FMRG: Cyber) Summer Program, 2024 Cornell NanoScale Science & Technology Facility Research Experience for Undergraduates (CNF REU) Program*

*Principal Investigator(s): Dr. Nicholas Abbott, Dr. Rong Yang; Smith School of Chemical and Biomolecular Engineering, Cornell University*

*Mentor(s): Soumyamouli Pal, Shiqi Li; Smith School of Chemical and Biomolecular Engineering, Cornell University*



*Primary Source(s) of Research Funding: 2024 CBE FMRG: Cyber Summer Program, 2024 CNF REU Program via the National Science Foundation under Grant No. NNCI-2025233*



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*Summer Program Website: https://cnf.cornell.edu/education/reu/2024*

*Primary CNF Tool Used: Zeiss Supra Scanning Electron Microscope*


## Abstract:

The ability to create designed polymer particle shapes would greatly benefit many applications, including timed drug delivery and reconfigurable metamaterials because the polymer's intrinsic properties largely depend on the shape. Prior works from our research group have leveraged the use of an anisotropic medium, namely liquid crystals (LCs), as templates to direct the growth of polymer structures by initiated chemical vapor deposition (iCVD) [1]. In this work, we have successfully obtained a range of glycidyl methacrylate (GMA) and divinyl benzene (DVB) polymer morphologies in a one-step, one-pot polymerization process by iCVD in a nematic LC called E7 (a eutectic mixture of cyanobiphenyls). We established multiple substrate temperatures in a single polymerization run by leveraging a thermal gradient placed directly on a cooled reactor stage. A filament array above the stage radially heats the gradient, providing lower temperatures as the distance from the gradient to the filament increases. E7 has a nematic to isotropic phase transition temperature of ~ 60°C, above which the orientational order of the LC mesogens no longer exists. We have investigated the effect of temperature on the rate of evaporation and phase change of the LC by utilizing a brightfield and cross-polarized optical microscope placed directly over the reactor for in-situ monitoring. Using a set of controls and experiments, we have mapped a set of reactor conditions where temperature solely influences the progression of particle morphology, allowing us to study how the morphology varies with temperature. These conditions limit the amount of evaporation and prevent isotropic phase change of the LC. Structural characterization using the Cornell NanoScale Facility Zeiss scanning electron microscope reveals the formation of different particle morphologies as a function of the various temperatures achieved.


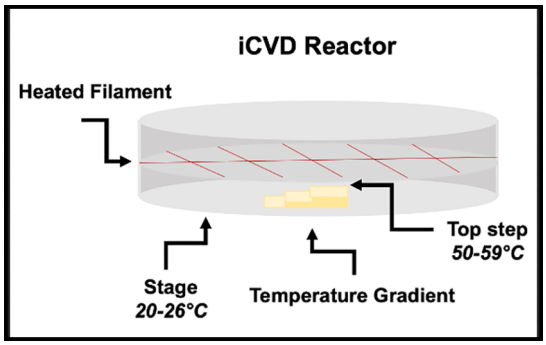


*Figure 1: Schematic of the temperature gradient in the iCVD reactor.*

## Summary of Research:

Micro and nanoparticles are promising for future imaging, medical, and energy applications. The ability to synthesize and control the size and morphologies is crucial for utilizing these particles at an industrial scale. Initiated chemical vapor deposition (iCVD) is a promising technique for synthesizing nanoparticles since it allows for high control of continuous polymerization and provides multiple particle morphologies without external manipulation. We utilized liquid crystals (LCs) as an anisotropic medium to provide a template for the iCVD polymerization and to optically monitor the polymerization in-situ using a long-distance focal lens. Our work focused on determining the effect of temperature on the morphology of glycidyl methacrylate (GMA) and divinyl benzene (DVB) polymeric particles polymerized using the iCVD-in-LC system.

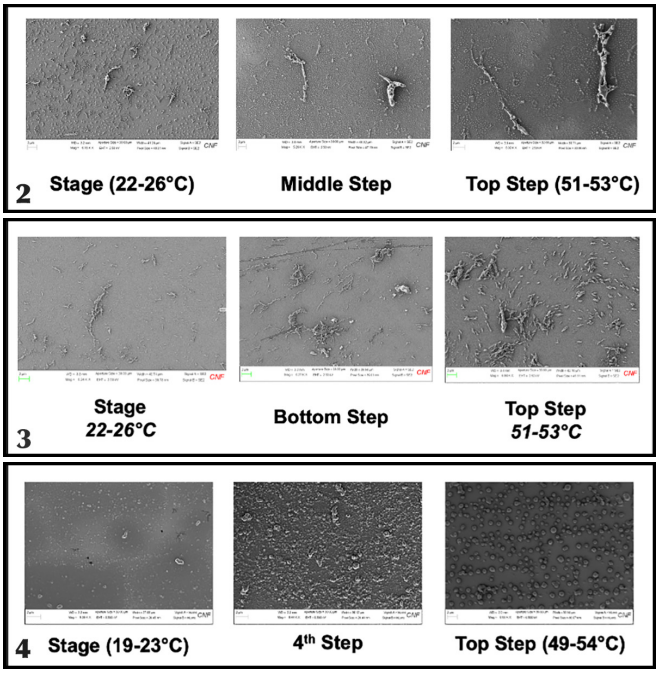


*Figure 2: Morphologies of GMA particles polymerized on OTS. Figure 3: Morphologies of GMA particles polymerized on glass. Figure 4: Morphologies of DVB particles polymerized on OTS.*

Utilizing a temperature gradient placed in the iCVD reactor, we achieved multiple temperatures within one polymerization run, as shown in Figure 1. The gradient was created by stacking glass slides in a staircase fashion. The reactor stage was cooled using a chiller set at 5°C, and a heated filament array was set above the reactor stage, reaching ~ 260°C. Our custom-built staircase sample holder experiences higher temperatures at the top step and lower temperatures at the bottom. We mapped the top step and reactor stage temperatures and consistently achieved a temperature difference of 20-25°C between the two extremes. We achieved multiple temperatures during each reactor run by placing samples on different steps of the staircase sample holder. This allowed us to compare the morphologies of the GMA particles polymerized in LC at different temperatures while minimizing the variables that could contribute to morphological differences. LCs are sensitive to temperature and change phase as temperature increases. The LC nematic phase provides mesogen orientational order and is the iCVD polymerization target phase. As temperature increases, the LC mesogens will transition to the isotropic phase; at this point, the LC loses its order and does not provide a templating effect. E7 LC was used for this project and has a nematic to the isotropic phase transition of ~ 60°C. To ensure the E7 remained in the nematic phase, we monitored multiple steps on the staircase and found no phase change of LC in the samples placed on any step during 30-minute and 60-minute polymerizations.

We also utilized two surfaces for the iCVD reactions: nochromix-treated glass and octadecyltrichlorosilane (OTS) substrates. Cross-polarized optical images of the LC samples were taken before and after the polymerization. We found negligible evaporation and no phase change of the LC during the 60-minute polymerizations for both glass and OTS samples using the optical images and the long-distance lens placed directly above the reactor. However, an anchoring change was observed at the mid-range temperatures for OTS from homeotropic to planar/tilted LC anchoring. We are currently investigating the cause of the anchoring change. After the polymerization, we characterized the morphologies of the GMA particles using a Zeiss Supra scanning electron microscope. We found that the particle morphology for GMA particles on OTS and glass does not drastically change their morphology but instead becomes larger and more elongated, as shown in Figures 2 and 3.

Utilizing the temperature gradient, we also polymerized DVB particles on OTS. We found that DVB particle morphologies differ more significantly than GMA polymerized at similar temperatures, as shown in Figure 4. The lower temperatures provide 300-400 nm diameter DVB nanoparticles. As temperature increases, DVB particles become larger and less symmetrical; at higher temperatures, they become symmetrical microspheres 1 $\mu$m in diameter. We hypothesize that DVB can achieve more morphologies because of crosslinking, while GMA is linear, achieving fewer morphologies.

## Conclusion and Future Steps:

Using a temperature gradient, we achieved multiple temperatures during a single LC-templated iCVD reactor run, allowing the comparison of GMA morphologies at different temperatures. We found that the GMA morphologies do not differ significantly with increasing temperature but increase in size and elongation. DVB particles were also polymerized using the temperature gradient, and the obtained morphologies changed more significantly. Reproducible reactor runs must be done to ensure the GMA particles are fully characterized at the different polymerization temperatures. The temperature gradient created for this project can also be used in future polymerizations to achieve multiple temperatures within a single polymerization.

## Acknowledgments:

Thank you to CBE FMRG: Cyber and the CNF REU for all the funding and support I received during the 2024 summer. I also want to thank my mentors, Soumyamouli Pal and Shiqi Li, for their support and mentorship. Finally, thank you to my PIs, Dr. Abbott and Dr. Yang, for hosting me this summer and allowing me to work in their fantastic labs.

## References:

[1] Jain, A., Pal, S., Abbott, N. L., and Yang, R. (2023, March 10). Single-step synthesis of shape-controlled polymeric particles using initiated chemical vapor deposition in liquid crystals.

# Stoichiometric Dependence of Physical and Electrical Properties of Silicon Nitride


## CNF Summer Student: Daniel Teleshevsky
## Student Affiliation: Electrical and Computer Engineering, Cornell University



*Summer Program(s): 2024 Xing Army Educational Outreach Program (AEOP), 2024 Cornell NanoScale Facility Research Experience for Undergraduates (CNF REU) Program*



*Principal Investigator(s): Grace (Huili) Xing, Electrical and Computer Engineering, Cornell University*

*Mentor(s): Phil Infante, Cornell NanoScale Facility, Cornell University*



*Primary Source(s) of Research Funding: Xing Army Educational Outreach Program (AEOP), National Science Foundation under Grant No. NNCI-2025233*



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*Summer Program Website: https://cnf.cornell.edu/education/reu/2024*

*Primary CNF Tools Used: LPCVD Furnace, CVC SC4500 Thermal Evaporation System, FleXus, Woollam Spectroscopic Ellipsometer*


## Abstract:

In recent years, nitride transistors have received much attention in the semiconductor device research community due to their wide bandgap, high thermal conductivity, and polarization properties. Two important performance metrics of these devices are the suppression of leakage current through the gate dielectric and its resilience under repeated use. Previous studies [1] have shown that these properties can be improved in SiNx (a common gate dielectric for nitride transistors) by changing the stoichiometry of the dielectric deposition.

This investigation entails the physical and electrical characterization of silicon nitride (SiNx) thin films deposited on silicon substrates by low-pressure chemical vapor deposition (LPCVD). Films were deposited at temperatures of 775°C, 750°C, and 725°C, and dichlorosilane to ammonia gas flow ratios of 5:1, 5:2, and 1:4, yielding a total of nine samples. Physical characterization measurements, including stress and index of refraction, were conducted on each film. The films with the lowest Si content showed the most stress and lowest index of refraction. Aluminum contacts were deposited on the silicon nitride using CNF's CVC SC4500 Thermal Evaporation System and patterned by contact lithography in a metal-first process to form MOS capacitors.

Capacitance-voltage behavior of the fabricated capacitors was measured at a DC probe station to determine the dielectric properties of the SiNx. The leakage current through the capacitors under applied bias was also measured as a function of time to determine the time-dependent dielectric breakdown of each film.


## Summary of Research:

The goal of this research was to check the impact of low pressure chemical vapor deposition conditions on the characteristics of physical and electrical properties of silicon nitride. This was done using a parallel plate capacitor that consisted of silicon and aluminum as its plates, and silicon nitride as the dielectric. The physical properties tested included the stress imposed by the dielectric and the index of refraction of the dielectric. The electrical properties consisted of the dielectric breakdown of the dielectric, and capacitance measurements of some of the capacitors that included the dielectric.

The process began with a plain 100 mm n-type silicon wafer, on which silicon nitride was deposited using low pressure chemical vapor deposition (LPCVD). This deposition was done at three different ammonia to dichlorosilane ratios and at three different temperatures. The goal of these varying conditions being to vary the concentration of silicon in the dielectric. The three dichlorosilane to ammonia ratios were regulated using the LPCVD furnace, and these three ratios were 5:1, 5:2, and 1:4. The three different temperatures chosen were 775°C, 750°C, and 725°C. This process resulted in nine wafers that had distinct deposition conditions. The physical properties, such as stress and index of refraction, were measured using the FleXus and the Woollam Spectroscopic Ellipsometer respectively. The silicon nitride index of refraction increased with the concentration of silicon during deposition. The stress imposed by the silicon nitride decreased with an increasing silicon concentration, as well as with higher temperatures during deposition (Figure 2).

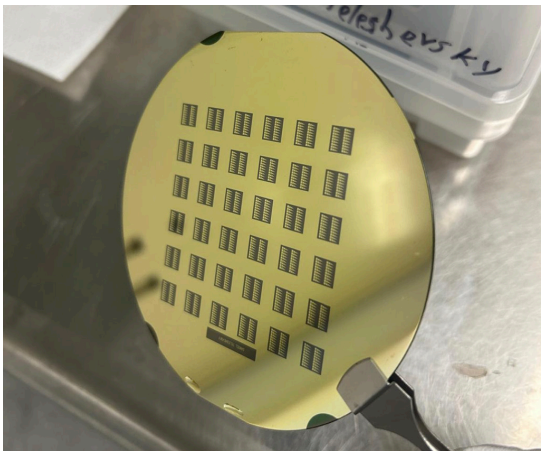

*Figure 1: Photograph of the wafer with the individual capacitors visible on the black squares.*

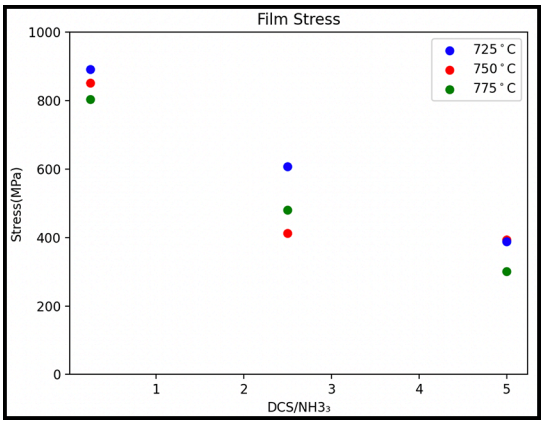


*Figure 2: Graph of the stress of the wafer, which is one of the physical properties measured. A potential downward trend of increased stress with decreased silicon concentration is depicted.*

Then, the wafer was coated with aluminum using thermal evaporation, which was patterned by liftoff using photolithography. This resulted in six clear square capacitors whose width was 50 $\mu$m, 100 $\mu$m, 200 $\mu$m, 300 $\mu$m, 400 $\mu$m, and 500 $\mu$m (Figure 1).

As part of the electrical characterization, the dielectric breakdown of these capacitors, as well as the capacitances of the 500 $\mu$m capacitors were measured using the Everbeing EB-6 DC Probe Station. This study included two variables, which were the flow rate of dichlorosilane to ammonia ratios, and the deposition temperature. The dielectric breakdown of silicon nitride was tested in all nine different wafers. It was found that films with a higher concentration of silicon broke down at lower voltages (Figure 3). Different deposition temperatures also showed to impact dielectric breakdown, with higher deposition temperatures causing a dielectric breakdown at lower voltages (Figure 4).

## Conclusions and Future Steps:

Both deposition temperatures and silicon content had an effect on the physical and electrical properties of the dielectric. Higher silicon content resulted in lower stress and a higher index of refraction, as well as a faster dielectric breakdown. Additionally, a higher deposition temperature resulted in lower stress and a faster dielectric breakdown. While both conditions did impact the properties of the film, silicon content had a greater effect than deposition temperature.

In the future, time-dependent measurements should be taken of the dielectric breakdown at each of the conditions, and this data should be collected in much larger quantities in order to conduct statistical analysis and determine the statistical significance of the data.


## Acknowledgements:

I would like to thank: the Army Educational Outreach Program and the Cornell NanoScale Facility Research Experiences for Undergraduates program; Professor Grace (Huili) Xing, my principal investigator, and Joseph Dill of the Jena-Xing group who provided me with scientific guidance throughout this project; as well as Phil Infante, my mentor, and Ben Infante, without whom this project would have been impossible.


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[1] W. M. Waller, et al., in Proc. CS-MANTECH, Indian Wells, CA, USA, May 2017.


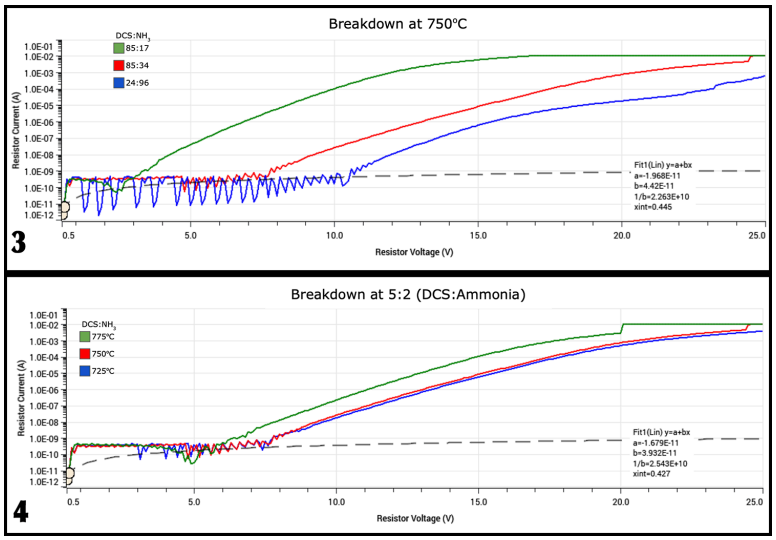


*Figure 3, above: Graph of the dielectric breakdown of the silicon nitride at 750°C. A trend of a faster breakdown at higher concentrations of silicon is demonstrated. Figure 4, below: Graph of the dielectric breakdown of the silicon nitride at a 5:2 dichlorosilane to ammonia deposition ratio. A trend of faster breakdown at higher deposition temperatures is demonstrated.*

# Atomic Layer Etching of III-Nitride Semiconductors


## CNF Summer Student: Hajo Johann Wise
## Student Affiliation: Mechanical Engineering, Rochester Institute of Technology

*Summer Program(s): 2024 Xing Army Educational Outreach Program (AEOP), 2024 Cornell NanoScale Facility Research Experience for Undergraduates (CNF REU) Program*

*Principal Investigator(s): Professor Huili Grace Xing, Electrical and Computer Engineering, Materials Science and Engineering, Cornell University*

*Mentor(s): Dr. Xinwei Wu, Cornell NanoScale Science and Technology Facility, Cornell University*



*Primary Source(s) of Research Funding: 2024 Xing Army Educational Outreach Program (AEOP), National Science Foundation under Grant No. NNCI-2025233*



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*Summer Program Website: https://cnf.cornell.edu/education/reu/2024*

*Research Group Website: https://jena-xing.engineering.cornell.edu/*

*Primary CNF Tools Used: Veeco Icon AFM, ABM Contact Aligner, Zeiss SEMS, Plasma-Therm Takachi ALE, Oxford 81 RIE etcher, Oxford 100 PECVD, P-7 Profilometer, Woolam RC-2 Ellipsometer*


## Abstract:

III-nitride semiconductors offer unique advantages in the manufacturing of high-voltage field effect transistors (FETS). However, production of nanoscale III-nitride FETs requires precise etching of III-nitride semiconductor films. We identified atomic layer etching (ALE) as an ideal technique for this application. ALE weakens the bond between a film and its surface layer via a chemical reaction with a reagent gas or plasma. The reagent is then purged, and the surface is bombarded with non-reactive ions. These ions impart enough energy to sputter away the reacted surface layer, but not enough to remove unreacted material underneath. These self-limiting characteristics allow for consistent removal of a few atomic layers at a time [1].

To adapt and characterize ALE for the processing of III-nitride films, samples with gallium nitride (GaN), aluminum nitride (AlN), and aluminum-gallium nitride (AlGaN) films were etched in the Cornell NanoScale Facility's (CNF) Plasma-Therm Takachi ALE tool. All ALE recipes tested used a $Cl_2$ and $BCl_3$ chemistry. However, key parameters such as gas flow rate, bias power, inductively coupled plasma (ICP) power, and step times were varied. Critical etch metrics such as surface roughness, film thickness, etch rate, and etch selectivity were recorded for each trial. By identifying recipe elements that yielded favorable etch results, this report gives preliminary guidance for the ALE of III-Nitride semiconductors.


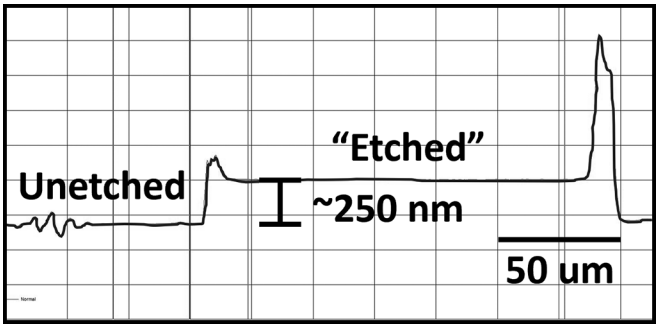


*Figure 1: Profilometry reading of "etched" feature.*

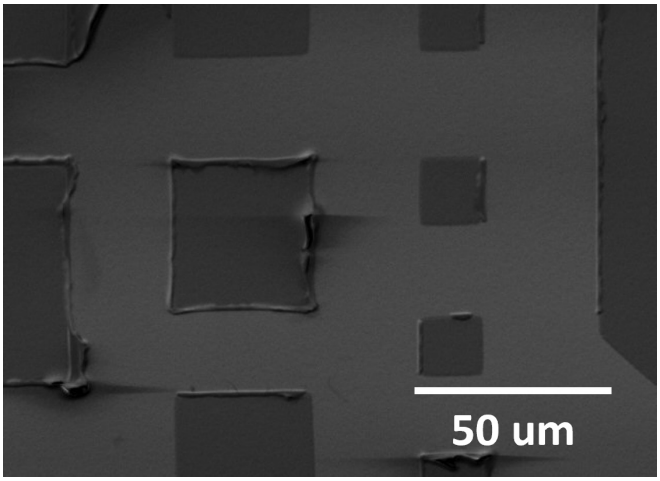


*Figure 2: SEM image of "etched" squares.*

## Summary of Research:

The first round of ALE processing was performed with one of each sample type (GaN, AlN, AlGaN) and a photoresist mask process. Nlof-2020 negative photoresist was chosen due to its popularity in device fabrication. Test features were patterned onto the samples to provide convenient etch characterization sites. The recipe flowed 30 sccm each of $Cl_2$ and $BCl_3$ for surface modification and applied 10 W of bias power for ion

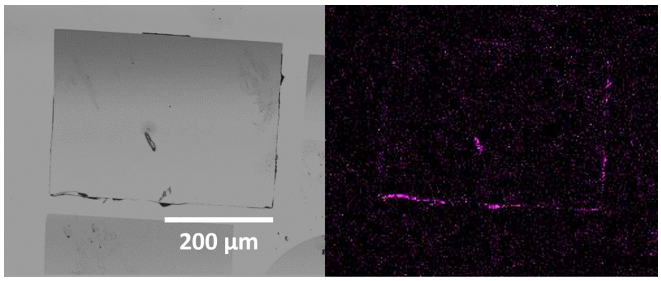


*Figure 3: SEM and boron EDS imagery of photoresist-masked sample.*

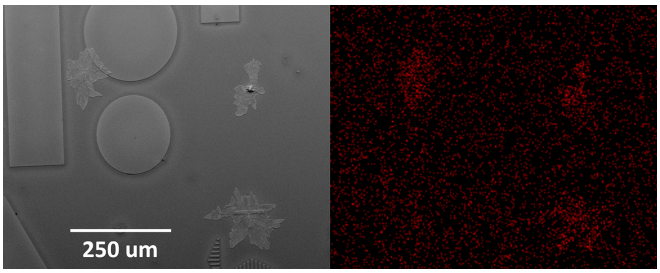


*Figure 4: SEM and chlorine EDS image of hard-mask sample, including crystalline defects.*

bombardment. All three samples were processed at the same time, for 20 ALE cycles.

Following ALE, profilometry was performed on the AlGaN sample, producing the reading shown in Figure 1. Notably, this reading indicated that the "etched" areas were ~ 250 nm higher than the unetched areas. This meant that something must have deposited during the etching process. This substance can be seen in SEM imagery of the sample (Figure 2), where the raised squares should be etched into the surface. Both the GaN and AlN samples exhibited deposition as well.

To identify the substance, energy-dispersive x-ray spectroscopy (EDS) was employed to map elements on the sample's surface. Figure 3 shows an SEM image of the AlGaN sample with a corresponding boron EDS map. Boron correlates with deposits along the edge of the etch pad, suggesting that it played a role in deposition. However, EDS is not sensitive enough to lighter elements to positively identify the material.

While inconclusive, the EDS results hinted that photoresist might play a role in the deposition. Consequently, our process flow was adapted to use an $SiO_2$ hard mask for the next trial. Only AlN was tested, due to limited sample availability. The ALE recipe was altered to flow 30 sccm of $Cl_2$ and 3 sccm of $BCl_3$, while the bias power was reduced to 8 W. These changes limited boron concentration, reducing the likelihood of adverse reactions. The sample was processed for 100 total ALE cycles, with measurements taken after 50 cycles.

Initial results from the hard-mask sample were promising, with ellipsometry indicating an etch depth of 20 nm after 50 cycles. The etched surface was also significantly smoothed, with a pre-etch roughness of 2.66 nm RMS and a post-etch roughness of 1.70 nm RMS. Unfortunately, the sample also exhibited crystalline defects across all exposed AlN surfaces. These defects are visible in the SEM image of Figure 4, where they appear to have grown across the patterned surface.

EDS was once again used to analyze the defects, with the EDS image Figure 4 showing a Chlorine map of the sample. Chlorine hotspots strongly correlate with the defects, indicating that they contain Chlorine. However, no other elements demonstrated a similar correlation. This poses an issue, as pure chlorine is a gas at room temperature. Logically, there must be other elements in the defects that we were unable to positively identify.

## Conclusions and Future Steps:

While ALE processing was not wholly successful, these trials highlight "best practices" that will hopefully contribute to a mature process flow in the future. The use of a hard mask is the most apparent, as it likely contributed to the significantly cleaner result of the second trial. Hard masks, especially $SiO_2$, are known for their resistance to unwanted chemical interaction. This is especially valuable for a high precision process like ALE, where even minimal unexpected reactions can disrupt the etching cycle.

Looking to the future, there are several promising approaches to obtain more favorable results. First, it would be useful to analyze the deposits with wavelength-dispersive x-ray spectroscopy (WDS). This technique is similar to EDS, but it offers increased sensitivity to lighter elements. This may allow for positive identification of the deposited materials, and subsequent process alterations to prevent their formation. Aside from WDS, an ALE recipe without $BCl_3$ would entirely remove a potential source of unwanted chemical reactions. We believe that these techniques and alterations will bring us one step closer to the successful atomic layer etching of III-nitrides.

## Acknowledgements:

This work was carried out at the Cornell NanoScale Science and Technology Facility, an NNCI member site supported by NSF grant no. NNCI-2025233. The opportunity to work at CNF was provided by the Army Educational Outreach Program. I'd like to give special thanks to Professor Grace Xing, Dr. Xinwei Wu, Wenwen Zhao, Jeremy Clark, Joseph Dill, Lynn Rathbun, and Melanie-Claire Mallison.

## References:

[1] K.J. Kanarik, S. Tan, and R.A. Gottscho. Journal of PhyChemLetters 2018 9 (16), 4814-4821 DOI: 10.1021/acs.jpclett.8b00997 Copyright 2018 by American Chemical Society.

# Fabricating Oxygen Managed and Thermally Robust Nb-Based Josephson Junction


## CNF Project Number: 2126-12
## Principal Investigator(s): Gregory David Fuchs
## User(s): Jaehong Choi

*Affiliation(s): Applied and Engineering Physics, Cornell University*



*Primary Source(s) of Research Funding: Air Force Office of Scientific Research*



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*Primary CNF Tools Used: PT770 etcher, AJA sputter deposition, Oxford 81 etcher, Primaxx vapor HF etcher, SC4500 Even-hour evaporator, GCA 6300 DSW 5X g-line wafer stepper, DISCO dicing saw, Heidelberg mask writer - DWL2000, Zeiss SEM*


## Abstract:

Superconducting Josephson junctions (JJs) are important building blocks of a quantum qubit for next-generation quantum communication and technology. Fabrication of JJs has been heavily relied on aluminum due to its long coherence time and high-quality native oxide. However, aluminum has a low critical temperature (Tc), which makes Al-based JJs susceptible to quasiparticle poisoning and have a limited operation frequency [1-3]. Niobium, on the other hand, has higher Tc and provide a wide range of operation frequency. We fabricate niobium-based JJs that can withstand high temperature with minimized oxygen diffusion, leading to qubits with long coherence times. To achieve this, we create JJs from a trilayer where AlOx is capped with an oxygen diffusion barrier and optimize the sidewall profile of JJs to mitigate loss.


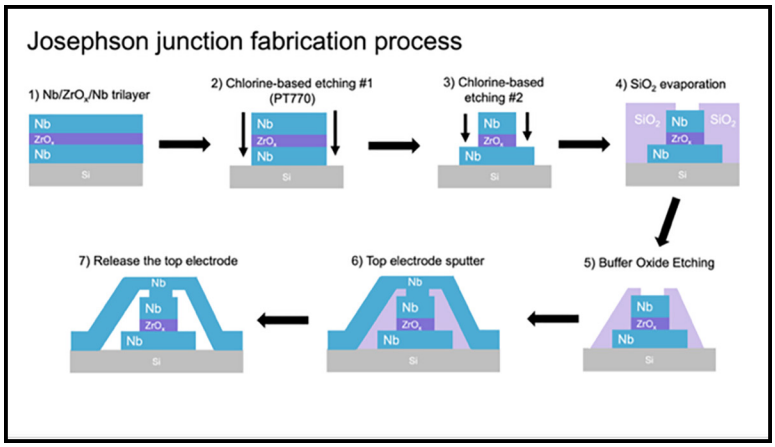


*Figure 1: Fabrication process of a Nb/ZrOx/Nb Josephson junction.*

## Summary of Research:

AlOx tunnel barrier suffers from chemical and thermal instability due to oxygen diffusion between the AlOx and electrodes, which can cause qubit decoherence. To mitigate this diffusion, we are capping AlOx with diffusion barrier. Materials with low heat of enthalpy such that it reduces the chemical gradient between AlOx and electrodes are good candidates for diffusion barrier. We are still in process of finding an optimal material for this diffusion barrier in collaboration within Cornell, and among Syracuse University and NIST-Boulder.

In the meantime, we start the fabrication process of the JJs to optimize etching process for sidewall characterization. We make JJs from a Nb/ZrOx/Nb trilayer. ZrOx is known to have good oxygen conservation [4], and we are going to compare its performance with that of a Nb/AlOx/Nb junction. We make junction geometry circular to allow sidewall access from any angles. Figure 1 summarizes the fabrication process. We use the GCA 6300 DSW 5X g-line wafer stepper to make a pattern of the junction. The junction diameter ranges from 2 $\mu$m to 9 $\mu$m within a device. Then, we use the PT 770 etcher for chlorine-based inductively coupled plasma (ICP) etching of the electrode and tunneling barrier. We evaporate the $SiO_2$ spacer layer after defining the mesa feature of the tunneling barrier. Subsequently, we sputter the top electrodes, which is followed by HF vapor etching of $SiO_2$ to release the top electrodes.

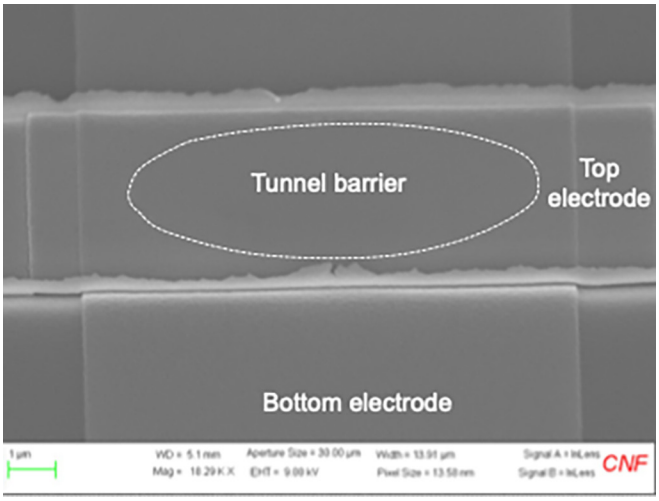


*Figure 2: SEM image of the Josephson junction after releasing the top electrode.*

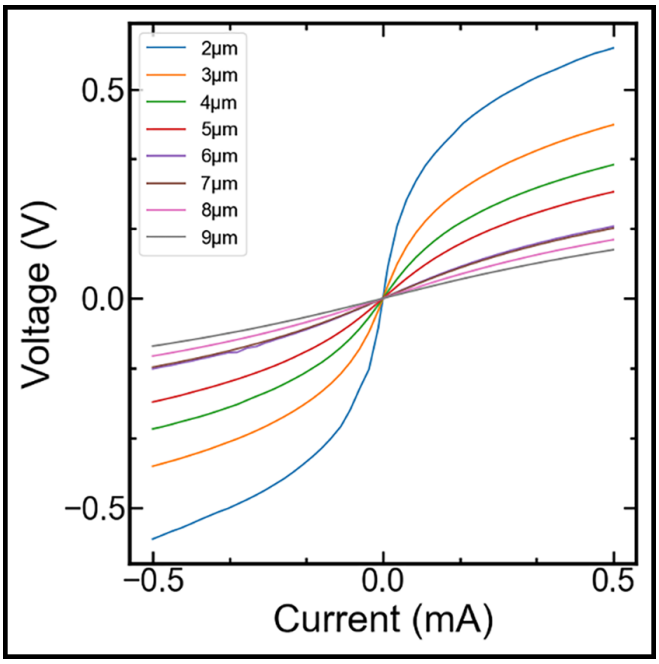


*Figure 3: Current-voltage (I-V) curve from Josephson junctions of various diameter, ranging from 2 μm to 9 μm.*

Figure 2 is an SEM image of the resultant Josephson junction. As shown in the image, lift-off residue persists despite multiple cycles of sonication. This is because sputtering is somewhat isotropic and not optimal for thick films. We can also see a gap between the top and bottom electrodes, indicating that the airbridge structure does not collapse after its release. We conduct four-wire voltage measurements by sourcing a current. Figure 3 is current-voltage (I-V) curves from the Nb/ZrOx/Nb JJs at room temperature. The I-V curves exhibit non-linear behavior, characteristic of tunnel junctions.

## Conclusions and Future Steps:

We successfully fabricated a Nb/ZrOx/Nb JJ with non-linear I-V characteristics. Next, we will fabricate a Nb/AlOx/Nb JJ and compare its performance with that of the Nb/ZrOx/Nb JJs. Also, once the optimal material for diffusion barrier is determined, we will cap AlOx with that material and test its performance.

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# Measuring Thickness of Extracellular Vesicle Mucin Coatings Using Nanoparticle Tracking Analysis

**CNF Project Number: 2272-14**
**Principal Investigator(s): Dr. Matthew Paszek**
**User(s): Erik Chow**

*Affiliation(s): Department of Biomedical Engineering, Cornell University*

*Primary Source(s) of Research Funding: National Science Foundation Graduate Research Fellowship*

*Contact: paszek@cornell.edu, ec829@cornell.edu*

*Primary CNF Tools Used: Malvern NS300 Nanosight*

## Abstract:

Extracellular vesicles (EVs) transport DNA, RNA, and proteins between cells and therefore have great potential as tools for disease diagnosis and therapeutics. The significance of the glycocalyx in EV biogenesis and function is largely unexplored, and the capacity to effect EV production and properties through rational manipulation of the glycocalyx remains poorly understood. We have previously demonstrated that overexpressing the mucin glycoprotein MUC1 in the glycocalyx leads to a dramatic increase in the production of EVs. Here, we characterize the innate MUC1 surface coatings on these "mucin-induced" EVs and demonstrate the ability to bioengineer mucin biopolymer coatings through genetically encoded coating thickness.

## Summary of Research:

Extracellular vesicles (EVs) have gained attention in numerous areas of biomedical engineering research — including disease pathogenesis and drug delivery, among others — for their ability to transport DNA, RNA, and proteins. The glycocalyx is a polymer meshwork of proteins, nucleic acids, and glycans which dictates numerous intercellular interactions, but its role in regulating EV biogenesis and function remains poorly understood. It has been previously shown that engineering the glycocalyx via the overexpression of mucin can result in membrane morphologies which are favorable for the formation of EVs [1]. This report summarizes research from the last year characterizing EV mucin coating thickness using nanoparticle tracking analysis (NTA).

MCF10A cells were genetically engineered to overexpress variable length, tetracycline-inducible MUC1 constructs with 0, 21, or 42 tandem repeats (TRs). Separately, cells expressing inducible MUC1 were genetically engineered for differential expression of glycosyltransferase or sialyltransferase enzymes to achieve variable MUC1 glycosylation. Specifically, GCNT1 overexpressing cells express MUC1 with more core II glycans; C1GALT1 KO cells express MUC1 with truncated glycans; or GNE KO cells express MUC1 with no glycans terminated by sialic acid. To induce MUC1 overexpression, cells were treated with 1 ug/mL doxycycline (Dox) for 24 h. Subsequently, cells were switched to serum-free media and cultured at 37 ., 5% CO2 for 15 h to 18 h. EV-containing media was harvested, and the EVs were isolated by PEG-enrichment according to an existing protocol [2]. EV mucin coatings were optionally removed by treatment with stcE mucinase [3], and EV sizes and concentrations were measured by nanoparticle tracking analysis (NTA) using the Malvern NS300 Nanosight.

Mucinase treatment of mucin-induced EVs resulted in a significant decrease in EV hydrodynamic radius (Figure 1). NTA of EVs from cells expressing variable-length MUC1 showed gradual increase in EV size correlated with mucin length, and significant increase in EV size was observed between EVs coated with MUC1 42xTR and those coated with MUC1 0xTR (Figure 2). Finally, mucin glycosylation had a measurable effect on EV coating thickness, with changes in EV size consistent with changes in parent cell glycocalyx thickness previously measured by scanning angle super-resolution microscopy [4] (Figure 3).

## Conclusions and Future Steps:

These studies demonstrate that EV properties can be dramatically impacted by the glycocalyx. Overexpression

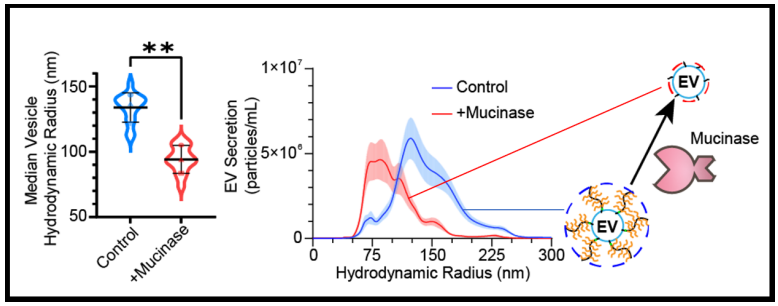


*Figure 1: Mucin-induced EVs have MUC1 surface coatings. Comparison of hydrodynamic diameter of EVs before and after treatment with StcE mucinase, (** = p < 0.01, Left). Size distributions of EVs from 1E7 cells before and after 100 nM StcE mucinase treatment measured by NTA. Plotted are the average particle concentrations +/-SEM from three independent experiments (Right).*

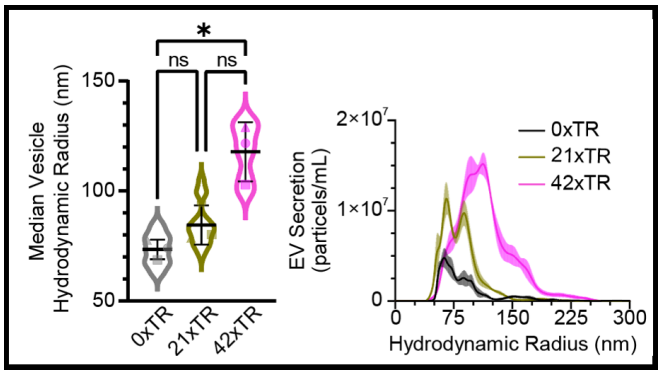


*Figure 2: Expression of variable length mucins has a correlated effect on EV coating thickness. Comparison of median hydrodynamic radius of EVs from cells expressing MUC1 with 0-, 21-, or 42xTR (Left). Data were collected from three independent experiments (* = p < 0.05). Size distributions of EVs. Plotted are average particle concentrations +/-SEM from three independent experiments (Right).*

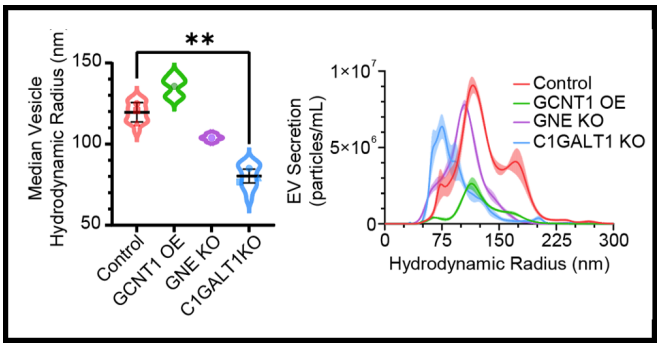


*Figure 3: Differential MUC1 glycosylation changes EV coating thickness consistent with changes in parent cell glycocalyx thickness. Comparison of median hydrodynamic radius of EVs from GCNT1 overexpressing, GNE KO, or C1GALT1 KO cells across three independent experiments (* = p < 0.05). Size distributions of EVs. Plotted are average particle concentrations +/-SEM from three independent experiments (Right).*

of MUC1 acts as a driver of EV release, and these EVs carry innate mucin surface coatings. Altogether, these data illustrate a synthetic biology approach to vesicle bioengineering by way of genetically encoded biopolymer coatings, which can be achieved either by direct manipulation of MUC1 biopolymer constructs or by genetic engineering of the EV parent cells to express mucins with varying glycosylation profiles. Future studies will assess the functional capabilities of mucin-coated EVs.

## References:


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# Polymer Film Microstructures via Surface-Directed Condensed Droplet Polymerization


## CNF Project Number: 2784-19
## Principal Investigator(s): Dr. Rong Yang
## User(s): Dr. Kwang-Won Park

*Affiliation(s): Smith School of Chemical and Biomolecular Engineering, Cornell University*



*Primary Source(s) of Research Funding: National Science Foundation (CMMI-2144171)*



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*Research Group Website: https://theyanglab.com*


*Primary CNF Tools Used: ABM contact aligner*


## Abstract:

Non-spherical polymer particles exhibit unique flow dynamics that enhance drug delivery by improving permeation through blood vessels walls. However, traditional synthetic methods are complex and inefficient. We developed a facile and scalable method called condensed droplet polymerization to address these challenges. In a chemical vapor deposition reactor, vaporized monomers condense onto a cold substrate, forming droplets that polymerize upon introduction of an initiator. Using a photoresist template with circular holes, we achieved monodisperse, hexagonally arranged polymer droplets. Removing the photoresist revealed concave-shaped polymers with potential nanoscale lens or drug delivery applications. This method offers precise control over particle size and morphology, paving the way for large-scale production and diverse biomedical applications.


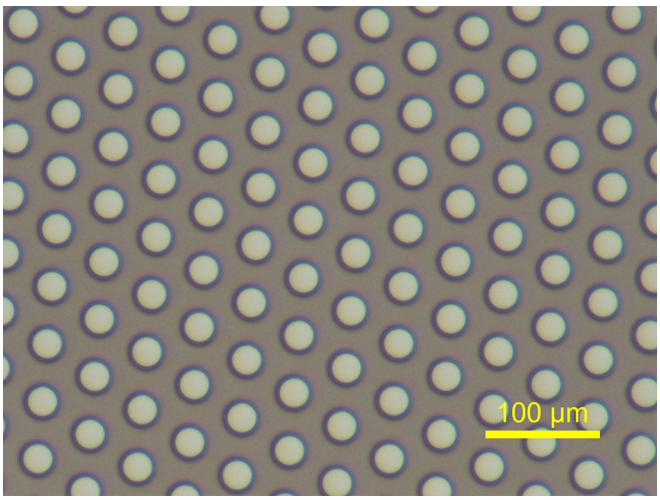


*Figure 1: Optical microscopy image of SPR220-4.5 photoresist with a hexagonal array of circular holes with 30 µm diameter.*

## Summary of Research:

Non-spherical polymer particles have shown great potential as drug delivery vehicles, exhibiting unique flow dynamics in blood vessels that enhance permeation through the vessel walls. However, the synthesis of non-spherical particles has been challenging due to complicated, time-consuming, and inefficient multi-step processes. Recently, our group demonstrated a facile and scalable synthetic strategy in the vapor phase, called condensed droplet polymerization [1].

In brief, within a conventional chemical vapor deposition vacuum reactor, vaporized monomer is introduced and subsequently condensed dropwise onto a cold substrate. These monomer droplets grow through continuous condensation and coalescence.

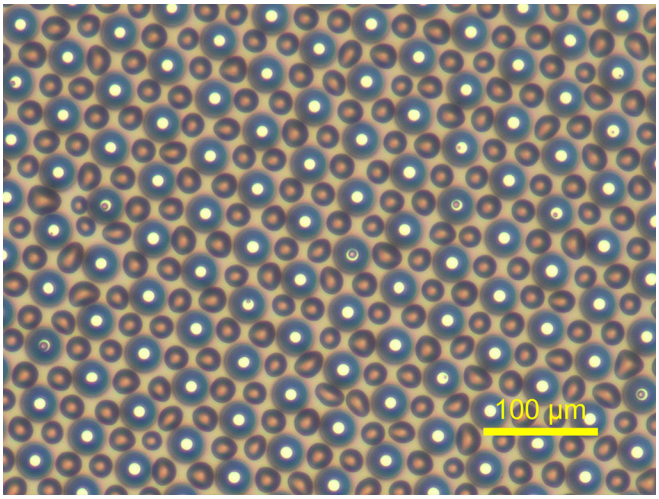


*Figure 2: Optical microscopy image of benzyl methacrylate monomer droplets condensed on the photoresist template shown in Figure 1.*

Once the droplet reaches the desired size, an initiator is introduced and decomposed into reactive radicals by heated filament arrays, initiating polymerization of the droplets. After a few minutes of polymerization (typically less than 2 minutes), the reaction is terminated by turning off the filament array and evacuating the reactor, resulting in polymer dome arrays. This CDP process has demonstrated that polymer particle size and morphology can be controlled and is suitable for large-scale production due to its rapid vacuum process. However, the random nature of condensation leads to a broad distribution of polymer particle sizes, which needs to be addressed. For drug delivery applications, the production of monodisperse polymer particles is critical to ensuring predictable and controlled drug release.

To address this issue, we created a template with an array of circular holes in the photoresist (Figure 1) and conducted the experiment using this template. The condensed droplet polymerization experiments confirmed that monomer droplets condensed simultaneously inside the holes and on the surface of the photoresist, regardless of the thickness of the photoresist (1 to 10 $\mu$m). As shown in Figure 2, when a densely packed hole array was used, we observed that monodisperse monomer droplets arranged themselves in a hexagonal pattern. This was an important result, demonstrating the potential to produce polymer domes of uniform size.

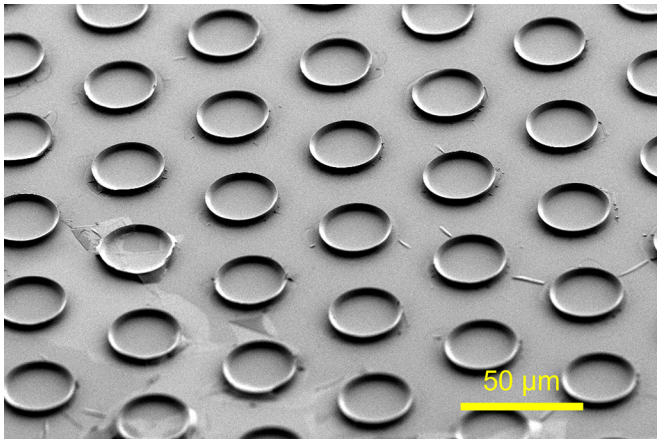


*Figure 3: Scanning electron microscopy image of poly(benzyl methacrylate) patterns on Si substrate.*

Interestingly, after completely removing the photoresist, the polymer formed inside the holes initially exhibited a concave shape due to the meniscus of the monomers (Figure 3). These polymer particles with such shapes are being closely monitored because they may exhibit nanoscale lens properties or unique drug delivery characteristics.

## Conclusions and Future Steps:

In conclusion, our study demonstrated the effectiveness of the condensed droplet polymerization method in producing non-spherical polymer particles with controlled size and morphology. By utilizing a photoresist template with an array of circular holes, we achieved monodisperse monomer droplet condensation and observed hexagonal arrangement patterns. These results highlight the potential of the process for large-scale production of uniform polymer domes, which are critical for drug delivery applications due to their unique flow dynamics and enhanced permeation properties. To build these findings, we are currently looking at further refinement of the patterned substrate design to enhance the uniformity of monomer droplet condensation, aiming for even more precise control over particle size, shape, and distribution.

## References:

[1] Franklin, Trevor, Danielle L. Streever, and Rong Yang. "Versatile and rapid synthesis of polymer nanodomes via template-and solvent-free condensed droplet polymerization." Chemistry of Materials 34.13 (2022): 5960-5970.

# Tuning the Surface Wettability of Alumina Membrane for Carbonate Crystallization


## CNF Project Number: 2983-21
## Principal Investigator(s): Dr. Greeshma Gadikota
## User(s): Akanksh Mamidala

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*Primary Source(s) of Research Funding: National Science Foundation Faculty Early Career Development Program (NSF CAREER)*



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*Research Group Website: https://gadikota.cee.cornell.edu/*


*Primary CNF Tools Used: Ramé-Hart Contact Angle Goniometer 500*


## Abstract:

Uncovering the nucleation and crystallization of calcium- and magnesium-carbonate in confined nanochannels is pivotal in interpreting the polymorph formation and stabilization in various physicochemical conditions having applications ranging from carbon sequestration to construction, plastics, and pharmaceuticals [1-3]. These carbonates exhibit anomalous physical and chemical phenomena due to finite size effects, and ionic effects altering their energies and kinetics of phase formation [4]. Accounting for these effects, the current research focuses on precipitating calcium- and magnesium-carbonate in confined alumina membranes and siliceous nanochannels having discrete pore sizes. Specifically, to account for the influence of surface wettability on carbonate growth, the alumina and siliceous nanochannels are transformed from hydrophilic to hydrophobic. This variation in surface wettability provides insights into the role of interfacial water on the growth/dissolution of carbonates. To probe and corroborate the synthesis of hydrophilic nanochannels into hydrophobic, a contact angle measurer was utilized and the mean contact angle of the hydrophilic and hydrophobic nanochannels was measured as 23.9° and 93.9°.


## Summary of the Research:

Understanding the influence of variation in surface wettability on carbonate growth and phase evolution is crucial and to alter the surface wettability the purchased anodic alumina membrane is first rinsed with ethanol and water and dried at 85°C for 30 minutes. Thereafter, the membranes were immersed in a solution of lauric acid in ethanol (20 g/L) for 15 minutes at 50°C and stirred at 120 rpm. The surface-modified membranes were again rinsed with ethanol and DI water and dried at 85°C for 30 minutes. This surface-altering process replaces the hydroxide moieties attached to the aluminum ion with lauric acid.

Contact angle measurement was performed using Ramé-Hart Contact Angle Goniometer 500 having a volume step of 10 .L and delay time of 4000 milliseconds to determine the surface wettability of the hydrophilic and hydrophobic surface. The contact angles measured were 23.6°, and 24.3° for the left side (.) and right side (.') of the droplet respectively

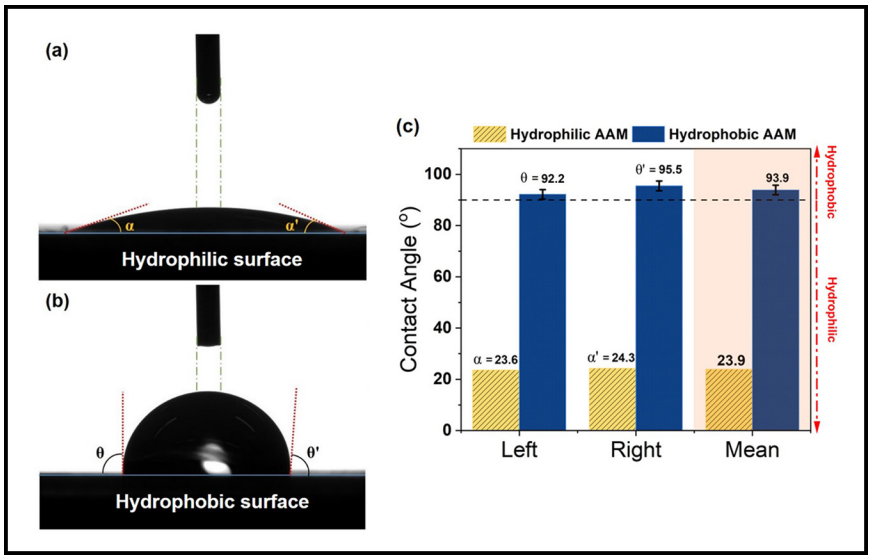


*Figure 1: Contact droplet angles.*

for the hydrophilic membrane and 92.2°, and 95.5° for the left side (.), and right side (.') of the droplet respectively for the hydrophobic membrane as shown in Figure 1. The mean contact angles were 23.9° and 93.9° for hydrophilic and hydrophobic anodic alumina membrane respectively. Based on the analysis, synthesis of the membrane from hydrophilic to hydrophobic was accomplished.

## Conclusion and Future Steps:

The behavior of fluids in nanoconfinement is an intricate mechanism characterized by anomalous phase behavior, spatial density profiles, and unique ion transport dynamics [4,5]. In this research, a similar mechanism is studied by analyzing the evolution of calcium- and magnesium-carbonate in nanoconfinement in different surface wettability environments. Before analyzing the phase evolution, synthesizing hydrophilic membranes into hydrophobic was performed using lauric acid, and to corroborate the hydrophobicity, a contact angle measurement was performed. The mean contact angle for the hydrophobic membrane attained was 93.9° validating the synthesis approach.

The future steps involve the transformation of anodic alumina membranes using lauric acid of different pore sizes and investigating the intricate relation between pore size and surface contact angle. Furthermore, the surface of silica nanochannels will be modified into hydrophobic using agents like sodium dodecyl sulfate (SDS), ethanol, methanol, etc. [6,7], and the contact angle for these membranes will be measured.

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# Lithography for Topological Nanowires

**CNF Project Number: 3032-22**
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**User(s): Han Wang**
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*Primary Source(s) of Research Funding: Semiconductor Research Corporation (SRC) JUMP 2.0 SUPREME*

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*Primary CNF Tools Used: JEOL 6300, PT 720 etcher, CVC SC4500 Combination Thermal/ E-gun Evap System, Zeiss Supra SEM, Nabity Nanometer PGS, YES Asher, Woollam RC2 Spectroscopic Ellipsometer*

## Abstract:

The resistivity scaling of copper interconnects with decreasing dimensions remains a major challenge in the continued downscaling of integrated circuits, which causes increased signal delay and power consumption in the circuits [1]. Therefore, new materials are needed for the next generation of interconnects beyond the 7 nm technology node. Topological semimetals like molybdenum phosphide (MoP), owing to their topologically protected surface states and suppressed electron backscattering, show promising resistivity values compared to copper interconnects at nanometer scale [2]. Here, with the assist of electron beam lithography and reaction ion etching, we successfully synthesized 1D topological MoP nanowires with tunable line width and thickness to investigate its resistivity scaling effect at nanometer scale.

## Summary of Research:

The fabrication flow chart of single crystalline topological MoP is shown in Figure 1. We start from commercially available single crystalline molybdenum disulfide ($MoS_2$) bulk crystals. Single crystalline $MoS_2$ flakes exfoliated from bulk crystals were placed on dry thermal oxide silicon wafer. These wafers were pre-patterned with alignment girds designed by our lab to locate flakes of interest (Figure 2a). First round of e-beam exposure was performed using JEOL 6300 to produce the dumbbell-shaped pattern as the mask of etching. Then, reactive ion etching was performed using PT720 etcher with $SF_6$ etchant to etch away $MoS_2$ in the exposed area, leaving the dumbbell-shaped $MoS_2$ with 1D wire in the middle (Figure 2b). $SF_6$ fluorinates top layers of PMMA, making them hard to remove by acetone. Therefore, $O_2$ plasma etching using the same tool was subsequently performed to remove the top layer of fluorinated PMMA. Then, using template-assisted chemical vapor deposition (CVD), the $MoS_2$ nanowire was converted to 1D MoP nanowire by reacting with $PH_3$ gas (Figure 2c). To deposit electrodes and measure the resistance, second round of e-beam lithography was done using Nabity-NPGS system to produce the electrode pattern. After descum in YES Asher, 10 nm chromium and 100 nm gold was deposited on the wafer as electrodes using SC4500 evaporator. After lift-off, the device was done and ready for measurement.

Figure 3 (a) shows the scanning electron microscope (SEM) images of the 1D topological MoP nanowire synthesized via the method described above with a line width of 80 nm (left) and 30 nm (right), separately. Figure 3 (b) shows the Raman spectra of the wires before and after conversion. Before conversion, the E12g and A1g peaks of $MoS_2$ can be clearly seen at 384 and 409 cm-1, respectively. After conversion, the two Raman modes of $MoS_2$ disappeared and one peak at about 402 cm-1 shows up, which is an indication of MoP according to the literature [3]. Wires with any other designated line width can be fabricated by changing the pattern arrangement, e-beam dose, or the etching time. Wires with different thickness can also be fabricated through choosing exfoliated $MoS_2$ flakes of different thicknesses. This method thus provides an excellent approach for fabricating 1D topological nanowires to investigate the unconventional resistivity scaling effect expected for them.

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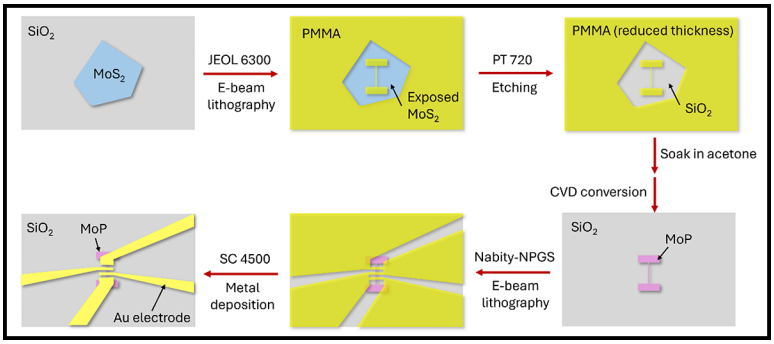


*Figure 1: Process flow of 1D MoP nanowires as well as the 4-point transport measurement devices.*

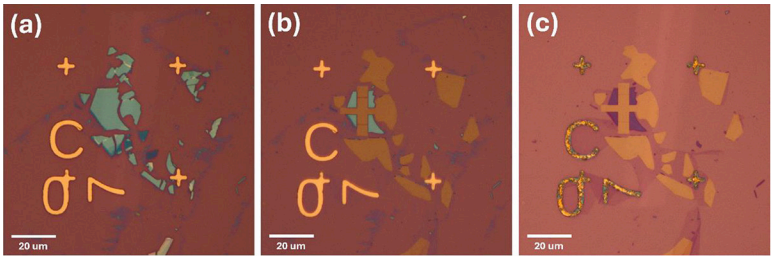


*Figure 2: (a) Exfoliated $MoS_2$ on the pre-patterned dry thermal oxide wafer. (b) Dumbbell shaped $MoS_2$ with 1D nanowires in the middle after e-beam lithography and etching. (c) 1D MoP nanowires after template-assisted CVD conversion from $MoS_2$.*

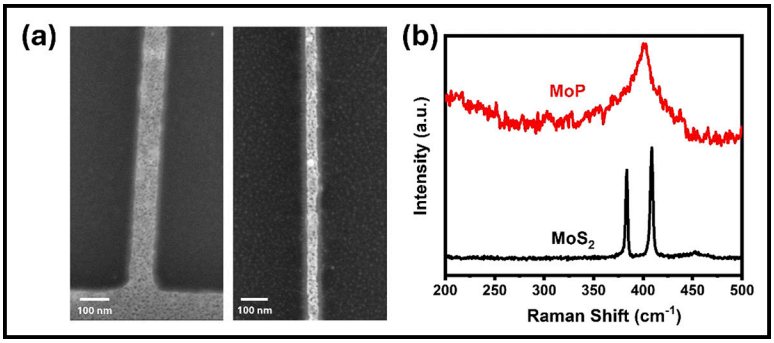


*Figure 3: (a) SEM images of 1D topological MoP wires with line width of 30 nm (left) and 80 nm (right). (b) Raman spectra of $MoS_2$ and converted MoP wires.*

# Through-Silicon Vias for Substrate-Integrated Waveguides

**CNF Project Number: 3078-23**
**Principal Investigator(s): James C. M. Hwang**
**User(s): Jin Hong Joo, Xiaopeng Wang, Yunjiang Ding**

*Affiliation(s): Department of Materials Science and Engineering, School of Electrical and Computer Engineering; Cornell University*

*Primary Source(s) of Research Funding: SUPREME Center funded by SRC/DARPA*

*Contact: jch263@cornell.edu, jj593@cornell.edu, xw569@cornell.edu, yd439@cornell.edu*

*Primary CNF Tools Used: ABM Contact Aligner, SUSS MA6-BA6 Contact Aligner, AJA Sputter Deposition – 1 & 3, UNAXIS 770 Deep Silicon Etcher, AJA Ion Mill, Zygo Optical Profilometer*

## Abstract:

As the demand for heterogeneous-integrated RF chips emerges, substrate-integrated waveguides (SIWs) based on through-silicon vias (TSVs) have become increasing important due to their low loss and high power capacity across a wide frequency range. In particular, above 110 GHz, SIWs are small enough to be integrated in Si interposers for high-power interconnects. They can also be used to form high-quality passive devices such as filters and antennas, which have been difficult to integrate on chip. This enables system on chip. In this study, we investigate the fabrication of SIWs in Si interposers with a thickness on the order of 100 um. The thin Si wafers were patterned and etched using the Bosch deep reactive ion etching (DRIE) process to create TSVs. Preliminary results indicate an etch rate of approximately 27 nm/s, which is too slow to etch through the Si interposer. Work is in progress to improve the etch rate.

## Summary of Research:

Silicon (Si) is most extensively used material in semiconductor devices due to its exceptional electrical and mechanical properties, including a high dielectric constant, electrical resistivity, breakdown strength and low loss tangent. These characteristics make it an attractive candidate for SIWs. However, its relatively low mechanical toughness and high thermal conductivity compared to materials like silicon carbide (SiC) pose challenges during processing, particularly in etching processes. Our group has successfully demonstrated SiC as a viable substrate material for SIW processing. The methodology developed for SiC SIW fabrication is adapted as a proof of principle for Si SIW fabrication.

To demonstrate the feasibility and develop a processing recipe for Si SIWs, we obtained a thinned high-resistivity Si wafer with a thickness of approximately 150 $\mu$m and resistivity of > 1000 ohm-cm. Drawing from a similar approach used for SiC SIWs, our methodology began with depositing a 50 nm layer of aluminum oxide ($Al_2O_3$) on the frontside of the Si wafer as an etch stop layer. This deposition was carried out using AJA Sputter Deposition – 1, achieving a deposition rate of approximately 2.8 Å/s.

Following this, the frontside was patterned using an ABM Contact Aligner, after which a titanium/aluminum (Ti/Al) layer was deposited using AJA Sputter Deposition – 2 to metalize the frontside. Concurrently, the backside of the wafer was patterned, and $Al_2O_3$ was deposited to define the etching pattern for TSVs. $Al_2O_3$ is chosen for its excellent masking properties in the Bosch DRIE process for Si, offering a selectivity as high as 1:1000.

For the DRIE, UNAXIS 770 Deep Silicon Etcher was used. To facilitate effective cooling during the reactive etching, the Si wafer was bonded to a sapphire carrier wafer using cool grease. The etching chemistry used was $C_4F_8/SF_6$, which reacts with and removes Si to create the vias anisotropically.

Using a Zygo Optical Profilometer, we repeatedly measured the depth of the TSVs and observed an etch rate of 3.3 Å/loop or approximately 27.3 nm/s throughout the process as shown in Figure 1.

Due to the fragility of the thinned Si wafer, precautions were taken during post-etching processes when removing cool grease and carrier wafer. Dicing streets were drawn on the Si wafer as shown in Figure 2, to facilitate simultaneous etching for easier detachment and dicing into smaller chips. Finally, the etch stop layer was physically removed using an AJA Ion Mill, and the backside was metallized with Ti/Al using AJA Sputter Deposition – 2 to fill the TSVs and establish connections to the frontside. The Si wafer after etching is shown


*Figure 1: Zygo Optical Profilometer image for TSV depth measurement.*

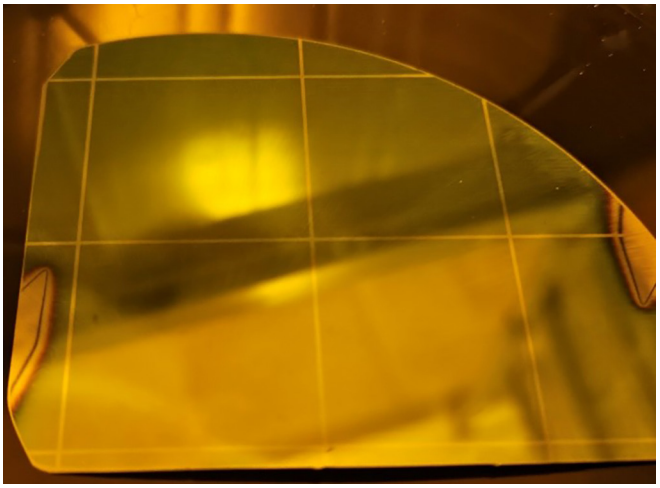

*Figure 2: Dicing street pattern on Si wafer.*

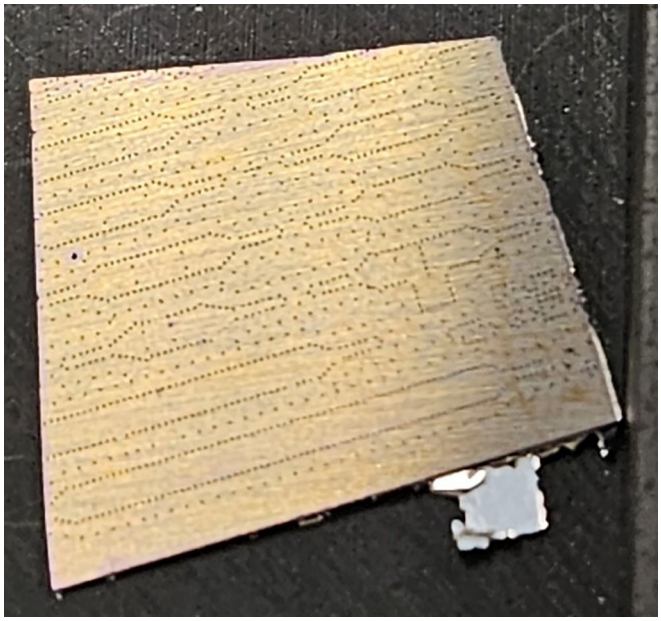

*Figure 3: Si SIW chip after the Bosch DRIE process.*

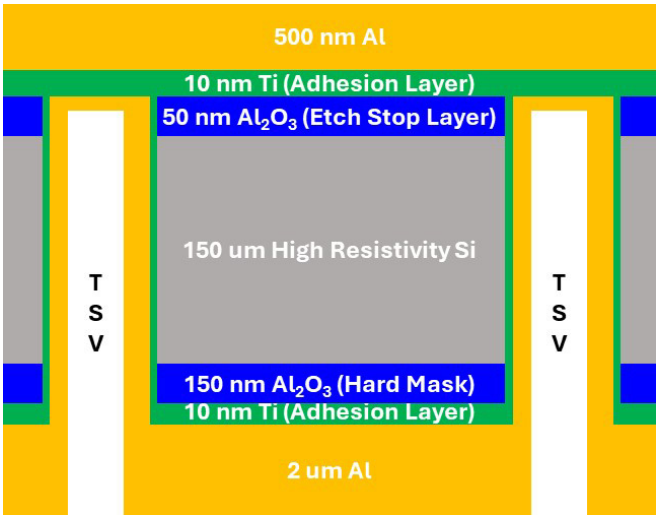


*Figure 4: Structure of Si SIW.*

in Figure 3 and the structural details and final product configurations are illustrated in Figure 4, showcasing the possibility of processing SIWs with thinned high resistivity Si wafers.

## Conclusion and Future Steps:

The fabrication of Si SIWs focused on studying the Bosch DRIE of thinned Si wafers, achieving an etch rate of 27 nm/s with uniform anisotropic etching across the wafer. With the etching process proven feasible, the next phase involves investigating the most effective methods and materials for metallizing the SIWs, particularly to fill the TSVs. Initially, atomic layer deposition (ALD) of platinum (Pt) is planned to coat the chip. Pt is chosen for its superior properties in enhancing interconnect reliability compared to Ti, which is prone to oxidation, potentially compromising device quality. Following the completion of processing steps, measurements will be conducted at the High Frequency Test Lab (HFTL) using the 220 GHz single-sweep probe station located at Cornell University. This comprehensive testing environment will provide critical insights into the performance and functionality of the fabricated SIWs at high frequencies.

## References:

[1] M. J. Asadi, L. Li, K. Nomoto, Y. Tang, W. Zhao, P. Fay, D. Jena, H. G. Xing, and J. C. M. Hwang. 2021 IEEE MTT-S Int. Microw. Symp. (IMS), Atlanta, GA, USA, 2021, pp. 669-672.

[2] D. Malta, E. Vick, S. Goodwin, C. Gregory, M. Lueck, A. Huffman, and D. Temple. 2010 IEEE International 3D Systems Integration Conference (3DIC), Munich, Germany, 2010, pp. 1-6.

# CNF NORDTECH Internship: Characterization of Oxynitride Films


## CNF Project Number: CNF Summer Internship
## Principal Investigator(s): Ron Olson, Lynn Rathbun
## User(s): Ben Infante

*Affiliation(s): Cornell NanoScale Science & Technology Facility (CNF), Cornell University*



*Primary Source(s) of Research Funding: Cornell NanoScale Facility (CNF), a member of the National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation (Grant NNCI-2025233)*



*Contact: olson@cnf.cornell.edu, rathbun@cnf.cornell.edu*

*Research Group Website: https://www.cnf.cornell.edu/*


*Primary CNF Tools Used: MRL Industries E4 Furnace*


## Abstract:

As part of the CNF NORDTECH internship program, various projects were worked upon this summer. One of the projects was the characterization of an oxynitride process using the MRL Industries LPCVD furnaces. The oxynitride film is heavily used in photonics, and specifically done to gather information for a remote request for the film. The characterization of the thin film involved varying the gas ratios in order to determine the effect of adding oxygen to the recipe. Other factors such as pressure, and temperature were kept constant. The time variable was flexible since the sample needed to be thick enough to gather the data. The main objective of the characterization was to determine the deposition rate, the index of refraction and the stress of the film. From the data gathered, a few conclusions were drawn. As the concentration of oxygen in the film increased, the index of refraction, the deposition rate, and the stress all decreased.


TABLE 1: MFC GASSES

| Mass Flow Controller | |
|---|---|
| NH3 | 200 sccm |
| N2O | 200 sccm |
| DCS | 150 sccm |

TABLE 2: CONSTANT PARAMETERS

| Constants | |
|---|---|
| Pressure | 200 mTorr |
| DCS % | 40% |
| DCS | 60 sccm |

## Experimental Procedure:

The oxynitride film was deposited using the Low-Pressure Chemical Vapor Deposition (LPCVD). In order to properly determine the effects of different gas ratios, many of the determining variables were kept constant throughout the experiment. These included the chamber pressure, and the dichlorosilane set percentage. For the gas flow settings, the mass flow controller (MFC) has a set amount of gas flow it can allow measured in standard cubic centimeters per minute (sccm). The gas ratios are a percentage of that flow. For the oxynitride run, there are 3 different gasses used to deposit the film. The gasses given are Ammonia ($NH_3$), Nitrous Oxide ($N_2O$) and Dichlorosilane (DCS). Using the gasses we can determine the constant parameters for the experiment. These gasses can be viewed in Table 1 and the constant parameters in Table 2.

TABLE 3: GAS FLOW PARAMETERS

| Wafer ID | Time | NH3 % | NH3 Sccm | N2O % | N2O Sccm |
|---|---|---|---|---|---|
| ON-1 | 30 | 90 | 180 | 0 | 0 |
| ON-2 | 30 | 90 | 180 | 0 | 0 |
| ON-9 | 30 | 80 | 160 | 10 | 20 |
| ON-10 | 30 | 80 | 160 | 10 | 20 |
| ON-11 | 30 | 70 | 140 | 20 | 40 |
| ON-12 | 30 | 70 | 140 | 20 | 40 |
| ON-13 | 30 | 60 | 120 | 30 | 60 |
| ON-14 | 30 | 60 | 120 | 30 | 60 |
| ON-15 | 30 | 50 | 100 | 40 | 80 |
| ON-16 | 30 | 50 | 100 | 40 | 80 |
| ON-17 | 60 | 40 | 80 | 50 | 100 |
| ON-18 | 60 | 40 | 80 | 50 | 100 |
| ON-19 | 60 | 30 | 60 | 60 | 120 |
| ON-20 | 60 | 30 | 60 | 60 | 120 |
| ON-21 | 60 | 20 | 40 | 70 | 140 |
| ON-22 | 60 | 20 | 40 | 70 | 140 |
| ON-23 | 90 | 10 | 20 | 80 | 160 |
| ON-24 | 90 | 10 | 20 | 80 | 160 |

From these initial parameters, a formulated experiment can be developed. Starting out by scribing our wafers, the gas ratios can be compiled. Silicon Nitride is formed using $NH_3$ and DCS. So that will become the start point. After the initial run the $NH_3$ percentage will decrease while the $N_2O$ percentage will increase. This pattern will be repeated until there is no $NH_3$ flow left, and the only gasses in the chamber are $N_2O$ and DCS. The specific gas flows used can be viewed in Table 3.

From this table, one of the most noticeable columns is the time column. Initially time was supposed to be held as a constant. But as the $N_2O$ percentage increased, the deposition rate decreased dramatically which will be showcased later in the results section. If the time was not increased, the thickness of the film would have been way too thin to gather any usable data.

## Results:

After each run was performed, the films were tested using the J. A. Woollam RC2 Ellipsometer. This was used to determine the thickness of the film, which would allow the deposition rate to be calculated. The ellipsometer also provided the index of refraction of the film. After the initial film properties were gathered, the film on the back side of the wafer was etched, to make a stress measurement using the FleXus. This allowed for the film to generate stress on only the top side of the wafer, so the stress of the film can be measured. Before the furnace process, each wafer was tested to determine an initial stress value. This can then be used to determine the stress of the film by taking the difference. The overall results can be viewed in Table 4.

TABLE 4: RESULTS

| Wafer ID | Time | NH3 % | NH3 Sccm | N2O % | N2O Sccm | Thickness | Dep Rate | Index | Stress |
|---|---|---|---|---|---|---|---|---|---|
| ON-1 | 30 | 90 | 180 | 0 | 0 | 100.37 | 3.345667 | 2.0174 | |
| ON-2 | 30 | 90 | 180 | 0 | 0 | 101.89 | 3.396333 | 2.0176 | |
| ON-9 | 30 | 80 | 160 | 10 | 20 | 90.73 | 3.024333 | 1.994 | |
| ON-10 | 30 | 80 | 160 | 10 | 20 | 91.35 | 3.045 | 1.994 | |
| ON-11 | 30 | 70 | 140 | 20 | 40 | 80.2 | 2.673333 | 1.965 | |
| ON-12 | 30 | 70 | 140 | 20 | 40 | 79.04 | 2.634667 | 1.965 | |
| ON-13 | 30 | 60 | 120 | 30 | 60 | 70.19 | 2.339667 | 1.936 | 856.915 |
| ON-14 | 30 | 60 | 120 | 30 | 60 | 69.65 | 2.321667 | 1.935 | |
| ON-15 | 30 | 50 | 100 | 40 | 80 | 59.06 | 1.968667 | 1.90369 | 848.105 |
| ON-16 | 30 | 50 | 100 | 40 | 80 | 59.58 | 1.986 | 1.90474 | |
| ON-17 | 60 | 40 | 80 | 50 | 100 | 95.66 | 1.594333 | 1.87467 | |
| ON-18 | 60 | 40 | 80 | 50 | 100 | 96.59 | 1.609833 | 1.87606 | 677.133 |
| ON-19 | 60 | 30 | 60 | 60 | 120 | 92.59 | 1.543167 | 1.8689 | 732.999 |
| ON-20 | 60 | 30 | 60 | 60 | 120 | 90.93 | 1.5155 | 1.87191 | |
| ON-21 | 60 | 20 | 40 | 70 | 140 | 44.28 | 0.738 | 1.75273 | 619.534 |
| ON-22 | 60 | 20 | 40 | 70 | 140 | 45.33 | 0.7555 | 1.75518 | |
| ON-23 | 90 | 10 | 20 | 80 | 160 | 31.59 | 0.351 | 1.65041 | 321.178 |
| ON-24 | 90 | 10 | 20 | 80 | 160 | 32.2 | 0.357778 | 1.65213 | |

From the results we can observe the decrease in deposition rate, index of refraction and stress as a factor of the gas ratio. For the stress data, only one wafer was etched, to leave a complete wafer still intact for more possible further exploration such as etch tests etc. The first few wafers there were no stress data for, due to some errors with the furnace, that led to the tool needing maintenance. With the other data, a better visualization is provided in Figures 1 and 2.

The figures tend to show a very linear trend for the deposition rate, with one outlier at the 60 percent mark. A similar trend appears with the index. At this range the film possibly has a larger concentration of oxygen than nitrogen. The same point also shows an inverse exponential regression of the index of refraction. As the original few points are very linear, at 60 percent $N_2O$, the index decreases rapidly. Overall the characterization will allow users to better produce certain films to their specifications. Consistent characterization of tools allows for more accurate results based on the tool information sheets. With tools going down, and requiring maintenance, the results of a process may change over time. This experiment should allow users to produce an accurate oxynitride film to their specifications.

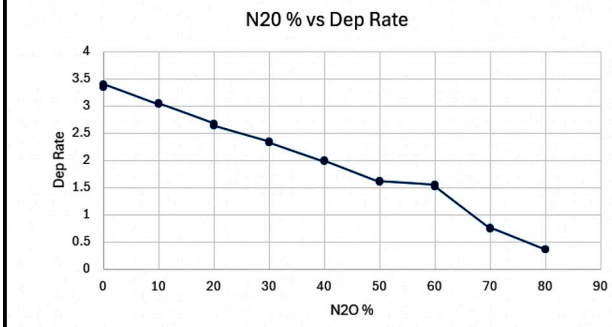


Fig. [1]: N2O% Vs Dep Rate

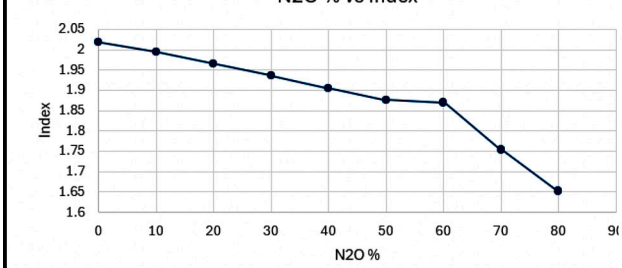


Fig. [2]: N2O Vs Index

# Nanotechnology Workforce and Curriculum Development


## CNF Project Number: CNF Summer Internship
## Principal Investigator(s): Ron Olson[1], Lynn Rathbun[1]
## User(s): David M. Syracuse[2]

*Affiliation(s): 1. Cornell NanoScale Science and Technology Facility (CNF), Cornell University; 2. Tompkins-Seneca-Tioga Board of Cooperative Educational Services (TST BOCES)*



*Primary Source(s) of Research Funding: Cornell NanoScale Facility (CNF), a member of the National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation (Grant NNCI-2025233)*



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*Research Group Website(s): https://www.cnf.cornell.edu/, www.mistersyracuse.com*


*Primary CNF Tools Used: Unaxis 770 Deep Silicon Etcher, ABM Contact Aligner, Hammatech Wafer Developer, Anatech Plasma Asher*


## Abstract:

Nanotechnology, and all of the promises and penitential that it holds, is becoming increasingly important from an economic, workforce. Microprocessors, computer memory, and other technologies that make modern life possible all depend on research and development at the nanoscale. It is therefore critical that more people are exposed to possible careers and ideas surrounding this concept. While it is important to ensure that current employment needs in this field are met, it's critical that we look toward the future of the industry. This requires students in K-12 educational programs to be well-versed in these concepts and ideas. I worked to make sure that teachers, students, and industry partners are working together to achieve these goals.


## Summary of Research:

## Curriculum Development:

The New York State Science Learning Standards (NYSSLS) are being rolled out progressively, with 2026 as the target date for a complete transition away from the previous standards, which have been in place since 1996.1 In the intervening thirty years, there have been new discoveries from animals to elements that have reshaped how humans interact with their world. Chief among these is an explosion in the possibilities that nanotechnology can offer.

The new standards, while commendable, do not explicitly call out nanoscale concepts. For example, while there are performance expectations at all grade levels around engineering design, none of them are specifically relevant to solving problems at the nanoscale. There are also expectations at all grade levels for students to build devices that transform one type of energy into another, but again, nothing is mentioned about the scale. This presents an opportunity to include nanoscale examples where older, macroscale examples might have been previously used.

Dr. Tamer Uyar in the fiber science department studies a process called electrospinning, whereby a polymer is extruded from a needle via an electric field. Varying the voltage, humidity, or a number of other factors can change the size of the nanofibers that are produced. I worked with Dr. Uyar this summer to develop ways that this technology can be demonstrated in the classroom, and will continue to do so over the course of this academic year.

Because nanotechnology is inherently cross-curricular, it's also the ideal vehicle to deliver instruction that highlights the crosscutting concepts that the NYSSLS emphasize at every level. Most practicing scientists realize that a working knowledge of chemistry, physics, math, and myriad other subjects is necessary to grow our collective understanding and make progress in any field. To that end, I worked with and presented to in-service teachers through the United Federation of Teachers and the American Federation of Teachers to show them how nanoscale concepts can fit into their curricula.

I also presented at the Northeast Regional Defense Technology meeting at Rensselaer Polytechnic Institute on the value of creating and maintaining industry-education partnerships.

## Education and Outreach:

The goals of developing a competent and dynamic workforce for the burgeoning US semiconductor industry depend on students being knowledgeable of and interested in the field. To that end, I worked with students at several outreach events, including a Micron chip camp and two visits from students from New York City. These students came away with an appreciation for the complexity of the devices that are around them every day, as well as the possibilities for future education and employment in the field. I also gave tours to incoming first-year Cornell undergraduate students and to first-year graduate students. These tours gave a comprehensive perspective on what the CNF can offer in terms of research possibilities.

Because not all students or workers have access to a facility like CNF or the programs that it offers, I worked to help develop virtual reality (VR) modules that teach about important concepts in nanoscale manufacturing.

## Workforce Development:

A shifting economy requires a nimble workforce in order to be sustainable. The United States has invested in this ideal through initiatives like the CHIPS act, which, among other things, aims to bring more semiconductor manufacturing and job force training back to the country. In service of this, workforce development needs to happen on two main fronts: retraining of people already in the workforce, and preparation of students who will be entering it in the future.

I worked with the New York State Department of Labor to show them the mismatch between current educational programs and the needs of the semiconductor workforce, and will continue to work with them as one of many options to disseminate our virtual reality content.

## Microfluidic Device Fabrication:

While students can understand commercial microprocessors and the tools and methods used to produce them, their small size, immense complexity, and sensitivity to contaminants makes them difficult to work with the K-12 setting. Microfluidic devices are fabricated with identical techniques on identical substrates, but are much more forgiving. It's also possible to interact with them outside a cleanroom and on a scale that is smaller, but familiar, to most students. They therefore provide an ideal method to engage students with nanofabrication techniques in a way that allows for easy measurement and interaction with equipment already present in most science labs.

I have prepared several microfluidic devices that students can use to explore concepts related to the NYSSLS, and also use as jumping-off points for other concepts in a wide variety of STEM courses.

## References:

[1] https://www.nysed.gov/curriculum-instruction/science-implementation-roadmap-and-timeline.

# Cornell NanoScale Facility High School Summer Internship


## CNF Project Number: CNF Summer Internship
## Principal Investigator(s): Ron Olson, Lynn Rathbun
## User(s): Elyas Talda, Julius Won

*Affiliation(s): Cornell NanoScale Facility, Cornell University*



*Primary Source(s) of Research Funding: Cornell NanoScale Facility (CNF), a member of the National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation (Grant NNCI-2025233)*



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*Primary CNF Tools Used: Oxford 81, Oxford 82, ASML DUV Stepper, P7 Profilometer, Zeiss Supra SEM, Unaxis 770 Deep Silicon Etcher, Plasma-Therm Versaline Deep Silicon Etcher, Oxford Cobra ICP Etcher, Gamma Automatic Coat-Develop Tool*


## Abstract:

Our internship was mainly spent between two projects: characterization of multiple different tools and cleanroom upkeep, maintenance, and development. We helped to install new gas lines for compressed air and house nitrogen in an upstairs lab space. We also assisted in orbital welding a new exhaust pipe to a cleanroom etcher. Our other main project was working towards characterizing many different etch recipes on multiple Reactive Ion Etching (RIE) tools. We ran various etches, measuring the feature step-heights after pre-etch, etch, and cleaning processes. Late in our data-collection, we realized our measurements were incorrect when we calculated negative process selectivity rates. We attribute this error to noise in our larger measurements registering as larger than the change in photoresist height, potentially caused by multiple issues in our process. While we are disappointed by this, we have learned much about the levels of exactitude required in the cleanroom as well as how to consider acceptable margins of error and stay within them.


## Summary of Research:

Our characterization project focused on running etch recipes on multiple tools throughout the lab and measuring pre-, during-, and post-process step-heights. We could then take that data, calculate etch rates and selectivity, and compare it to previously collected data to determine how each tool functioned now versus in the past. This could illuminate tool issues or determine needed recipe adjustments as tools age.

Our characterization happened in several waves. In the first, we grew silicon nitride, silicon oxide, and polysilicon layers on silicon wafers before spinning photoresist and exposing and developing our pattern.

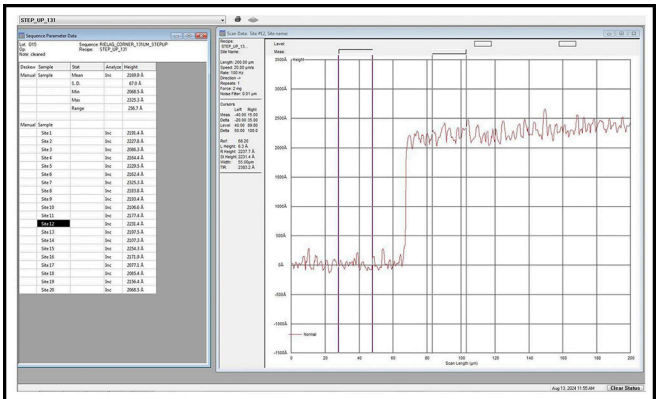

Figure 1: Noisy P7 Profilometer Data on an Oxide Wafer.

*Figure 2: Compressed Air (left) and House Nitrogen Gas Lines Ran in Lab 238. We installed six of these valves and their pipework under Paul's supervision.*

We then performed an anti-reflective coating (ARC) etch on each wafer before using the P7 Profilometer to measure the step-height of our pattern's features. We utilized a measurement sequence that took step-height measurements at 20 different locations across the wafer's surface to characterize the selectivity of each tool. Afterwards, we ran various etch recipes on the wafers using both the Oxford 81 and 82 (Table 1). After using the P7 to measure the post-etch height, we conducted a photoresist clean on the wafers before performing a final post-process measurement on each wafer.

In the second wave, we performed a similar process with bare silicon wafers using the Unaxis 770 Deep Silicon Etcher, the Oxford Cobra ICP Etcher, and the Plasma-Therm Versaline Deep Silicon Etcher (Table 2). Our process was identical to the first wave, beginning with an ARC etch, moving to the characterization etch, and ending with a photoresist clean, though this wave, we ran recipe duplicates. We used the same sequence on the P7 to measure each wafer after ARC etch, characterization etch, and clean. Unfortunately, we eventually determined that much of our data was unusable towards characterization due to noise in our measurements appearing larger than the change in photoresist height (Figure 1). This resulted in a negative selectivity rate.

We also decided to duplicate the processes done on the Oxford 81 and 82 in a third wave of wafers. This would not only fill in some data gaps from the first wave, but also provide us with a second set of data points to verify our findings. This third wave data, however, also proved to be critically mismeasured, again containing measurement noise that obscured the change in photoresist height. Many small issues with our measurements could have caused the overlarge noise, including problems in our sample loading, unseen profilometer needle slant, and a lack of clear parameters for acceptable data results, causing overlarge margins of error. We are disappointed by these nonresults; yet we have learned much through our mistakes. We have gained key knowledge on how to avoid small inaccuracies and mismeasurements that can sum into critical issues by clearly defining acceptable error margins and catching errors as they appear.

Additionally, we assisted Paul Pelletier, Senior Process Engineer, in many different tasks around the cleanroom, its service chassis, and other CNF lab spaces. We began working with him as he introduced us to the basics of high-purity gas line welding and cutting. We helped him weld and install a new exhaust line with a removable section for the Oxford 100 ICP Dielectric Etcher. Upcoming research in the CNF cleanroom will involve analyzing chemical compounds found in etching tool exhausts, making a removable exhaust necessary. Paul also gave us an introduction in working with copper and stainless-steel piping when we installed compressed air and house nitrogen lines above the ceiling in a second-floor lab space (Figure 2). We learned to fit, bend, and cut these pipes as well as how to analyze a space and think creatively around problems.

| Recipe Name | RF Power (Watts) | CF4 Flow Rate (sccm) | CHF3 Flow Rate (sccm) | SF6 Flow Rate (sccm) | Ar Flow Rate (sccm) | O2 Flow Rate (sccm) | Oxide Wafers Run | Nitride Wafers Run | Polyoxide Wafers Run |
|---|---|---|---|---|---|---|---|---|---|
| CF4 | 150 | 30 | | | | | 1 | 1 | 1 |
| CHF3+Ar | 200 | | 45 | | 15 | | 1 | | |
| CHF3+O2 Oxide | 150/200 | | 50 | | | 2 | 1 | | |
| CHF3+O2 Nitride | 150 | | 50 | | | 5 | | 1 | |
| Si anISO 100 mm | 100 | | 26 | 26 | | 17 | | | 1 |

Table 1: Oxford 81 and 82 Recipes and Wafers Ran. Note that the CHF3+O2 Oxide recipe ran at 150 watts on the Oxford 82, while the 81 ran at 200.

| **Tool** | Unaxis | Unaxis | Versaline | Cobra |
|---|---|---|---|---|
| **Process** | 0trench | Photonics | IAT | HBr+Ar PR 2 |
| **Time/Loops** | 80 loops | 5 mins | 100 loops | 10 mins |

Table 2: Etch Recipes Ran on Each Deep Silicon Etcher.

## Conclusions and Future Steps:

Our time as interns at CNF has been a great learning experience and engaging job for both of us. Working at a well-established facility with such experienced and knowledgeable staff is an opportunity that most don't get, much less directly after high school. Though the summer was short, we learned many different skills, from tool-operation and handling to report-writing and professional interaction. We also learned much about handling mistakes and unexpected outcomes, developing our response and correction skills. On a broader scale, CNF was both our first in-depth introductions to microelectronics and nanoscale work. We walk away from this internship with increased knowledge of what it means to work in the nanoscale field and the many opportunities it holds, information that may impact our futures as we head into our first year of college and beyond.

## Acknowledgements:

Special thanks to; Ron Olson, Ben Infante, Phil Infante, Jeremy Clark, Tom Pennell, Stacy Clementson, Paul Pelltier, and Sam Wright, for all their work in supporting us throughout our internship.

# The Effects of Nitrogen Annealing on Etch Rates of HDPECVD and PECVD Silicon Dioxide Films


## CNF Project Number: Cornell NanoScale Facility Staff Research
## User(s): Aaron Windsor

*Affiliation(s): Cornell NanoScale Facility, Cornell University*



*Primary Source(s) of Research Funding: National Science Foundation under Grant No. NNCI-2025233*



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*Primary CNF Tools Used: Plasma-Therm Takachi HDP-CVD System, Oxford Plasmalab System 100 PECVD, Woollam RC2 Spectroscopic Ellipsometer, Anneal LPCVD Furnace Tube, Verteq 1800.6 Spin Rinse Dryer*


## Abstract:

Plasma-enhanced chemical vapor deposition (PECVD) is a reliable technique for depositing silicon dioxide ($SiO_2$), but these films are notably less dense than thermal oxidation. It has been proposed that as-deposited PECVD films are composed of 5% by volume of micropores [1]. Over time, this porosity becomes susceptible to humidity, affecting stress and device performance. To collapse these micropores and improve film quality, PECVD $SiO_2$ films are often thermally annealed after deposition. While there is an abundance of information on annealing PECVD films, little has been published about films deposited/annealed by high density plasma enhanced chemical vapor deposition (HDPECVD). Unlike the weak ionization produced by PECVD capacitive plasma systems, HDPECVD generates high density plasma with an inductively coupled plasma (ICP) source coiled around the deposition chamber. This denser plasma increases free electron/precursor interactions which gives HDPECVD the advantage of operating with lower gas flows and at lower pressures than PECVD. The ICP power combined with wafer biasing gives HDPECVD the unique capability of depositing $SiO_2$ at 100°C. This work will compare the effects nitrogen annealing on HDPECVD and PECVD $SiO_2$ films by examining changes in film thickness and wet etch rates.

The SiO2 etch reaction in pure hydrofluoric acid (HF) is the combination of the following two reactions:

- $SiO_2 + 6HF \rightarrow H_2SiF_{6(aq)} + 2H_20$
- $SiO_2 + 3HF_2^- + H^+ \rightarrow SiF_6^{2-} + 2H_20$

With concentrations of pure HF lower than 10M, the fluoride ($F^-$) and bifluoride ($HF_2^-$) ions are the dominant etch species with the bifluoride etching silicon dioxide 4.5 times faster than HF [2]. Etching silicon dioxide in pure HF is rapid and is used for completely removing the oxide or the native oxide without damaging the silicon wafer. For a more controllable silicon dioxide etch used in semiconductor processing, buffer oxide etch (BOE) is preferred. The addition of ammonium fluoride ($NH_4F$) with HF suppresses the difluoride resulting in the HF complex becoming the dominant etch species [3].


## Summary of Research:

For this work, approximately 1000 nm of $SiO_2$ was deposited on single side polished N-type, 100 mm diameter, 525 $\mu$m thick, prime, <100> silicon wafers. For HDPECVD, all ten depositions were completed on a Plasma-Therm Takachi HDP-CVD System at the as-deposited temperature of 100°C with silane ($SiH_4$) and oxygen ($O_2$) precursor gases. For PECVD, an Oxford Plasmalab System 100 PECVD tool was used to deposit $SiO_2$ on nine wafers at an as-deposited temperature of 350°C with $SiH_4$ and nitrous oxide ($N_2O$). All wafers were MOS cleaned and nitrogen annealed from 300-1100°C for one hour. The anneal temperatures were calibrated from the combination of three separate heating elements in a low temperature chemical vapor deposition (LPCVD) furnace tube. A Woollam RC2 Spectroscopic Ellipsometer was used for all thickness measurements. The percent change in film thicknesses was calculated by the difference in as-deposited/annealed thicknesses divided by the as-deposited thickness and expressed as a percentage.

Wafers were submerged into room temperature (approximately 20°C in the temperature-controlled CNF cleanroom) 6:1 BOE at thirty-seconds intervals. After thirty seconds, the wafers were immediately submerged in deionized wafer and rinsed again using a Verteq 1800.6 spin rinse dryer. Three wafers were etched at a time and a new BOE solution was used after each three-wafer etching cycle. Wafers were etched process side up

to prevent any bubbles from effecting the etch results and the position of the wafers (top, middle and bottom) was rotated in the Teflon® wafer holder after each etch. Etching measurements were done after each thirty-second etch and ended after the oxide was etched below 150 nm. Etch rates were determined by averaging the differences in thicknesses after each thirty second etch. For comparison, the etch rate for LPCVD thermally wet oxide grown at 1100°C was calculated using this same method.

All the oxide films decreased in thickness when annealed, but the percentage change in thickness after annealing was significantly higher for HDPECVD films (Figure 1). As annealing temperatures increase above 400°C for PECVD oxide, remaining hydrogen from the silane precursor breaks down leaving extra micropores. Higher temperatures will collapse free hydrogen and as-deposited micropores and above 600°C, Si-O bonds will relax and become more ordered [4]. The relaxation of the PECVD oxide is apparent above 700°C, but the HDPECVD densification curve is different due to the lower temperature, gas flows and operating pressure required for the deposition. Denser films and reduced porosity resulted in lower 6:1 BOE etch rates as annealing temperatures increase (Figure 2). When annealed at 1100°C, both films had comparable etch rates to thermal oxide grown at 1100°C (Table 1). From both graphs, trends in annealing temperature densifications correlate with etch rate non-linearities. Future work should examine changes in the absorbance spectra of annealed Si-O networks from both deposition methods.

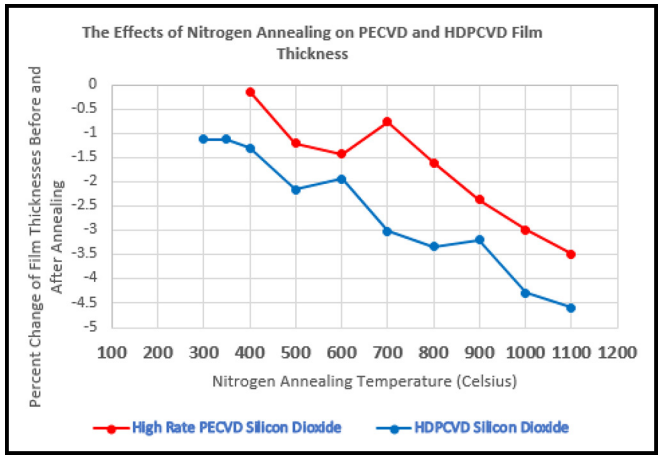


*Figure 1: Changes in $SiO_2$ thicknesses as nitrogen annealing temperatures increase for PECVD and HDPECVD films.*

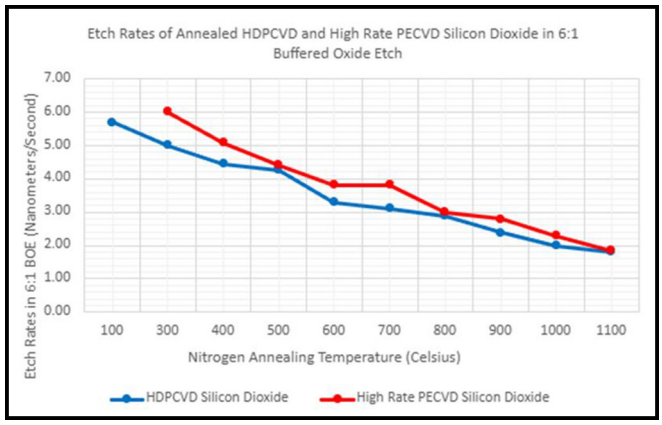


*Figure 2: Changes in $SiO_2$ etch rates as nitrogen annealing temperatures increase for PECVD and HDPECVD films.*

| $SiO_2$ Films | Etch Rate (nm/min) |
|---|---|
| High Rate PECVD Annealed @ 1100°C | 1.86 |
| HDPCVD Annealed @ 1100°C | 1.85 |
| Wet Thermal Oxidation @ 1100°C | 1.76 |

*Table 1: Etch rates for $SiO_2$ deposited or grown films @ 1100°C.*

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# The Effects of Nitrogen Annealing on Stress of HDPECVD and PECVD Silicon Dioxide Films


## CNF Project Number: Cornell NanoScale Facility Staff Research
## User(s): Aaron Windsor

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*Primary Source(s) of Research Funding: National Science Foundation under Grant No. NNCI-2025233*



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*Primary CNF Tools Used: Plasma-Therm Takachi HDP-CVD System, Oxford Plasmalab System 100 PECVD, Woollam RC2 Spectroscopic Ellipsometer, Flexus 2320-S Stress Measurement System, Anneal LPCVD Furnace Tube*


## Abstract:

While thermal oxidation is the most common method for batch processing silicon dioxide ($SiO_2$), the high thermal energy required (800°C -1200°C) and low deposition rates limits its use in modern semiconductor fabrication. In the late 1960's, the emergence of plasma enhanced chemical vapor deposition (PECVD) revolutionized the semiconductor industry. An inert plasma can dissociate precursor gases and provide the activation energy necessary to deposit thin films at temperatures between 200°C -450°C. Along with higher deposition rates, PECVD became a reliable method for depositing many dielectrics, but this process does not produce the same $SiO_2$ film quality as thermal oxidation. Typically, $SiO_2$ films have a moderate compressive stress which is beneficial for integrated circuit processing [1], but over time, humidity and ambient moisture will cause the stress to drift and become more compressive [2]. Controlling film stress and wafer flatness directly impacts the long-term quality of devices and excessive stress can lead to buckling or delamination. To stabilize stress, PECVD $SiO_2$ films are often thermally annealed after deposition to collapse micropores and breaks down bonded hydrogen (H) and hydroxyl groups (OH) [3].

Optimizing PECVD deposition parameters seems to be an alternative path for improving film quality, so in early 2022, the CNF installed a Plasma-Therm Takachi High Density Plasma Chemical Vapor Deposition (HDPECVD) system for depositing silicon oxide. This HDPECVD system uses an inductively coupled plasma (ICP) source to create a denser plasma than other conventional parallel plate PECVD systems such as our Oxford Plasmalab System 100. The higher density plasma translates into more free electrons to interact with reactive gas species, eliminating the need for high process gas flows. Combined with the capability of biasing the wafer, HDPECVD can deposit high quality films at significantly lower temperatures. While there is an abundance of information on PECVD films, little has been published about films deposited/annealed by HDPECVD. This work will compare the effects nitrogen annealing has on HDPECVD and PECVD $SiO_2$ film stress and wafer flatness.


## Summary of Research:

For this work, approximately 1.0 $\mu$m of $SiO_2$ was deposited on single side polished (SSP) N-type, 100 mm diameter, 525 $\mu$m thick, prime, <100> silicon wafers. For HDPECVD, all ten depositions were completed on a Plasma-Therm Takachi HDP-CVD System at the as-deposited temperature of 100°C with silane ($SiH_4$) and oxygen ($O_2$) precursor gases. For PECVD, an Oxford Plasmalab System 100 PECVD tool was used to deposit $SiO_2$ on nine wafers at an as-deposited temperature of 350°C with SiH4 and nitrous oxide ($N_2O$). All wafers were MOS cleaned and nitrogen annealed from 300-1100°C for one hour. The anneal temperatures were calibrated from the combination of three separate heating elements in a low temperature chemical vapor deposition (LPCVD) furnace tube. A Woollam RC2 Spectroscopic Ellipsometer was used for all thickness measurements before and after annealing. Stress measurement calculations were based on these thicknesses. All the oxide films decreased in thickness when annealed, but the percentage change in thickness after annealing was significantly higher for HDPECVD films. Film stress and wafer bow were measured on a Flexus 2320-S Stress Measurement System. Measurements were at room temperature using a 670 nm laser light source and at the zero- and ninety-degree (0° and 90°) orientation.

## Results:

The average as-deposited compressive stress at both orientations for HDPECVD $SiO_2$ was -235 MPa which is almost one-hundred MPa higher than the as-deposited PECVD oxide (-136 MPa). Both oxide films became less compressive (more tensile) as annealing temperatures were increased to 600° C, and more compressive at higher annealing temperatures (Figure 1). While the PECVD stress curve peaked at -32 MPa before becoming more compressive, the HDPECVD oxide annealed at 350° C had almost zero stress (-0.74 MPa) and films became tensile when annealed between 400°C - 700°C. At 1100°C, both films had a similar compressive stress (HDPECVD @ -244MPa and PECVD @ -246 MPa).

Wafer bow is an indicator of the flatness of a wafer in semiconductor processing. A compressive film will have a positive wafer bow and a tensile film will have a negative. New SSP wafers had an average wafer bow of -1.3 $\mu$m at the 0° orientation and -1.76 at 90° orientation. The average as-deposited wafer bow was higher for the HDPECVD films (+21.3 $\mu$m at 0° and +20.9 $\mu$m at 90°) which correlates with the higher compressive stress than the PECVD oxide (+12.3 $\mu$m at 0° and +12.1 $\mu$m at 90°). As with the stress, wafer bow changed significantly more negative (tensile) for the HDPECVD $SiO_2$ than the PECVD (Figure 2). Wafer bow was between +/- 3$\mu$m for $SiO_2$ annealed at 300°C, 350°C and 800°C for the HPCVD and from 500°C -700°C for PECVD $SiO_2$.

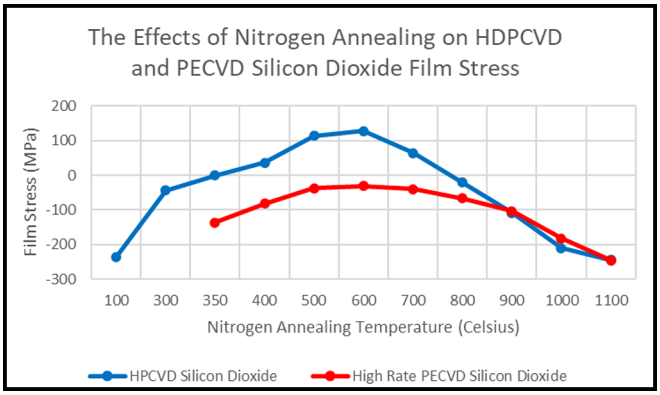


*Figure 1: Changes in $SiO_2$ stress as nitrogen annealing temperatures increase for PECVD and HDPECVD films.*

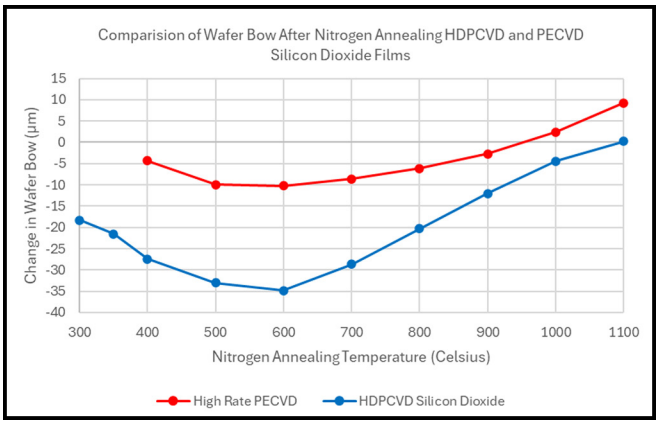


*Figure 2: Changes in $SiO_2$ wafer bow as nitrogen annealing temperatures increase for PECVD and HDPECVD films.*

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# The Viability of 1,3,3,3-Tetrafluoropropene as a Low Global Warming Potential Silicon Dioxide Etch Gas at the Cornell NanoScale Facility


## CNF Project Number: Cornell NanoScale Facility Staff Research
## User(s): George McMurdy, Jeremy Clark, Robert G. Syvret, Aaron Windsor, Ron Olson

*Affiliation(s): Cornell NanoScale Facility, Cornell University; EFC Gases & Advanced Materials*

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*Primary CNF Tools Used: Oxford Plasmalab System 100 ICP RIE system, FilMetrics F50-EXR Optical Measurement System, B2 Thermal Oxide LPCVD Furnace Tube*


## Abstract:

Silicon dioxide ($SiO_2$) is one of the most common dielectric materials in the semiconductor industry. Not only is $SiO_2$ an excellent insulator for integrated circuits and transistors, but it is also an effective hard mask and can be easily patterned at the microscale. While the ability to reactively ion etch (RIE) precise anisotropic features is vital for the future of the industry, many of the etch gases used are reactive hydrofluorocarbons (HFCs) which are considered greenhouse gases (GHGs). These gases hinder the earth's ability to cool down by absorbing/redirecting shortwave radiation from the sun and reflecting longwave radiation admitted from the earth's surface. For the past fifty years, climate scientists have been concerned that GHGs may have varying effects on the warming of the planet. In 1987, the Montreal Protocol was finalized to phase out the use and consumption of ozone depleting gases (OFCs) such as chlorofluorocarbons (CFCs) and bromofluorocarbons (halons) [1]. HFCs were once developed as replacements for OFCs but were later found to be warming the atmosphere at a faster rate than carbon dioxide [2] which is why in 2016, the Kigali Amendment was adopted to the Montreal Protocol to include limits on their use worldwide. Most recently, the United States Congress has taken further steps to reduce HFCs by enacting the American Innovation and Manufacturing (AIM) Act. This grants the U.S. Environmental Protection Agency (EPA) the authority to phase down eighteen HFC gases they consider having high Global-Warming Potentials or GWP.

The Aim Act wants the production and consumption of HFCs to be reduced by 40% between 2024–2028 and 85% by 2036 [1,3].

To reduce their consumption of HFCs while expanding chip manufacturing throughout the United States, the semiconductor industry is seriously exploring the next generation of lower GWP gases for etching semiconductors and dielectrics such as $SiO_2$.

The hydrofluoroolefin (HFO) 1,3,3,3-Tetrafluoropropene ($C_3H_2F_4$) has been recommended as a substitute gas for etching $SiO_2$. HFOs are considered a promising environmentally friendly replacement for CFCs, halons, hydrochlorofluorocarbons (HCFCs) and HFCs as refrigerants and for other industrial processes [4]. These gases have high gas phase reactivity along with exchange values (numerically equivalent of 100-year GWP) much lower than legacy etch gases such as trifluoromethane (HFC-23, $CHF_3$) and difluoromethane (HFC-32, $CH_2F_2$) [5].

This work will investigate the viability of the unsaturated fluorocarbon $C_3H_2F_4$ for etching $SiO_2$ when directly exchanged for difluoromethane, a known saturated fluorocarbon etch gas (both gases supplied by Electronic Fluorocarbons). Repeated blanket $SiO_2$ films were etched with both gases as a direct comparison of etch rates and uniformity on 100 mm wafers. Difluoromethane etches were done before and after repeated $C_3H_2F_4$ etches to examine possible unwanted side effects this HFO may have on the etch chamber and/or future etches.


## Experimental:

Approximately 500 nm of wet thermal oxide were grown on 100 mm diameter, 550 $\mu$m thick, single side polished, P-type prime silicon wafers. All dielectric etches were done on an Oxford PlasmaLab 100 inductively coupled plasma (ICP) RIE system that has dependable etched $SiO_2$ at the Cornell NanoScale Facility for over fifteen years. The etch parameter for both gases are illustrated

| Table 1: Etching Parameters for Silicon Dioxide | |
|---|---|
| $C_3H_2F_4$ or $CH_2F_2$ | 20 sccm |
| Helium | 80 sccm |
| ICP | 3000 W |
| RIE | 60 W |
| Chamber Pressure | 4 mTorr |
| Electrode Temperature | 10 °C |

| Table 2: 100mm Silicon Dioxide Etch Trials | | |
|---|---|---|
| Etch Gas Groups | Average SiO2 Etch Rate (nm/min) | Standard Deviation (nm/min) |
| First $CH_2F_2$ | 135.26 | 0.5 |
| $C_3H_2F_4$ | 160.85 | 1.1 |
| Last $CH_2F_2$ | 133.46 | 0.65 |

in Table 1. Both $C_3H_2F_4$ and difluoromethane were individually introduced through a gas ring just above the wafer on the electrode. Helium is applied for backside wafer cooling.

Blanket silicon dioxide thicknesses were mapped on twenty-four wafers and divided into three, eight wafer groups. The first group of eight wafers were etched consecutively with difluoromethane for ninety seconds and mapped again for thickness. The second group of eight wafers were etched for ninety seconds with $C_3H_2F_4$ and the third group of eight wafers were etched again with difluoromethane. Before all three etch groups, a ten-minute oxygen plasma chamber clean and seasoned for two-minute with either difluoromethane or $C_3H_2F_4$. Full wafer mapping and mean etch rates were calculated by measuring film thicknesses before and after etching using a FilMetrics F50-EXR Optical Measurement System. Each wafer map was measured at twenty-five points with 10 mm edge exclusion and aligned to the wafer's flat. The final average etch rates were calculated by the average of the mean etch rates for all eight wafers in a group.

## Results:

The full wafer etch test demonstrated that $C_3H_2F_4$ is an equivalent etch gas for $SiO_2$. The average mean etch rate is higher than difluoromethane (Table 2). The standard deviation was higher for $C_3H_2F_4$ than both difluoromethane runs. Further, the average etch rate was slightly lower and the standard deviation slightly higher for the last difluoromethane etch group than the first etch group. This demonstrates that a ten-minute oxygen clean is effective for cleaning the chamber after 720 seconds of $C_3H_2F_4$ etching and the unsaturated fluorocarbon does not display any obvious detrimental effects to the etch chamber or later etch processes. This first test was promising, but more work needs to be done in the future.

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[3] Environmental Protection Agency. (2024, January). Final Rule – Phasedown of Hydrofluorocarbons: Establishing the Allowance Allocation and Trading Program under the American Innovation and Manufacturing (AIM) Act. EPA. https://www.epa.gov/system/files/documents/2021-09/hfc-allocation-rule-nprm-fact-sheet-finalrule.pdf.

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# An Evaluation of 1,3,3,3-Tetrafluoropropene as a Low Global Warming Potential Silicon Dioxide Etch Gas at the Cornell NanoScale Facility


## CNF Project Number: Cornell NanoScale Facility Staff Research
## User(s): Aaron Windsor, Robert G. Syvret, Jeremy Clark, and Ron Olson

*Affiliation(s): Cornell NanoScale Facility, Cornell University; EFC Gases & Advanced Materials*



*Primary Source(s) of Research Funding: National Science Foundation under Grant No. NNCI-2025233*



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*Primary CNF Tools Used: Oxford Plasmalab System100 ICP RIE system, SUSS MicroTec Gamma cluster tool, ASML PAS 5500/300C DUV Wafer Stepper, Oxford PlasmaLab 80+ RIE System, SCE-110-RF Anatech Plasma Etcher, FilMetrics F50-EXR Optical Measurement System, Zeiss Ultra Scanning Electron Microscope, B2 Thermal Oxide LPCVD Furnace Tube*


## Abstract:

Currently, fluorocarbon (FC) and hydrofluorocarbon (HFC) gases are the primary choice for high aspect ratio etching of dielectric materials. The reason for this is that among the known and commonly used gases, one has access to a wide range of F:C ratios, e.g. from 4:1 in $CF_4$ to 1:1 in $CHF_3$, as well as great structural diversity including straight-chain and cyclic saturated alkanes (e.g., $CH_2F_2$ and $C_4F_8$), unsaturated alkenes (e.g., $C_3F_6$ and $C_5F_8$) and dienes (e.g., $C_4F_6$). These diverse characteristics provide a wealth of tunable options related to the aggressiveness of radical species generated in a plasma environment as well as, in some cases, important protective deposition properties of the resulting plasma fragments. Furthermore, each of the FC and HFC gases are readily available in high purity. However, despite all the positive attributes of FC and HFC gases, most have in common a serious downside, and that is related to their chemical and thermal stability. Most of the FC and HFC gases have a high global warming potential (GWP) and are damaging to the environment, and as a result, they are targeted for phase down and possibly eventual elimination through regulatory vehicles such as the U.S. AIM Act of 2021 [1].

One potential alternative to the use of FC and HFC gases is the use of low-GWP hydrofluoroolefins (HFOs). These HFOs have been developed by the fluorochemical industry and commercialized over the last decade or longer to replace high-GWP environmentally damaging refrigerants such as HFC-134a and foam expansion agents such as HFC-245fa. Amongst the known low-GWP HFOs one can find a range of F:C and H:C ratios. Thus, this group presents a potentially viable and environmentally friendly alternative to the use of legacy FCs and HFCs [2]. After promising initial tests etching blanket $SiO_2$ with the HFO 1,3,3,3-Tetrafluoropropene ($C_3H_2F_4$), the logical next step was to attempt real-world etches of patterned micron and submicron lines. This work will compare $SiO_2$ etches using the environmentally friendly alternative $C_3H_2F_4$ with saturated alkane legacy gases trifluoromethane (HFC-23, $CHF_3$) and difluoromethane (HFC-32, $CH_2F_2$).


## Experimental:

Approximately 500 nm and 1000 nm of wet thermal oxide were grown on 100 mm diameter, 550 $\mu$m thick, single side polished, P-type prime silicon wafers. All dielectric etches were done on an Oxford PlasmaLab 100 inductively coupled plasma (ICP) reactive ion etch (RIE) system. Both $C_3H_2F_4$ and $CH_2F_2$ were individually introduced through the gas ring just above the wafer on the electrode.

An automated SUSS MicroTec Gamma cluster tool and an ASML PAS 5500/300C DUV Wafer Stepper were used for all photolithography processing. Wafers were coated with approximately 62 nm of DUV 42P antireflective coating (ARC) followed by approximately 600 nm of DUV 210 positive photoresist, baked at 135°C for ninety-seconds and developed with AZ MIF 726 developer for sixty-seconds. Patterned etched features consisted of eight 5000 $\mu$m lines with widths between 5 $\mu$m and 300 nm. 40 $\mu$m x 400 $\mu$m "L" shaped corners were added to the CAD for the profilometer measurements. After development, each wafer was etched with an Oxford PlasmaLab 80+ RIE System to remove the ARC. A ten-minute oxygen plasma chamber clean and two-minute etch on a bare silicon wafer was done to season the chamber before etching with the process gas. For comparison, all three

| Table 1: $C_3H_2F_4$ Silicon Dioxide Etch Rates | | | |
|---|---|---|---|
| Etch Time (seconds) | Average $SiO_2$ Etch Rate (nm/min) | Average Resist Etch Rate (Angstrom/second) | Average Selectivity |
| 45 | 208.9 | 6.5 | 5.37 |
| 120 | 206.3 | 5.7 | 6.04 |
| 150 | 212.6 | 6.2 | 5.79 |
| 240 | 210.8 | 5.2 | 6.84 |

| Table 2: $SiO_2$ etch comparison between gases | | |
|---|---|---|
| Two-Minutes | | |
| Etch Gas Groups | Average SiO2 Etch Rate (nm/min) | Selectivity |
| $C_3H_2F_4$ | 206.3 | 6.04 |
| $CHF_3/O_2$ | 182.5 | 1.51 |
| $CH_2F_2$ | 158.7 | 2.24 |
| Four-Minutes | | |
| Etch Gas Groups | Average SiO2 Etch Rate (nm/min) | Selectivity |
| $C_3H_2F_4$ | 210.8 | 6.84 |
| $CHF_3/O_2$ | 181.3 | 1.55 |
| $CH_2F_2$ | 158.4 | 2.63 |

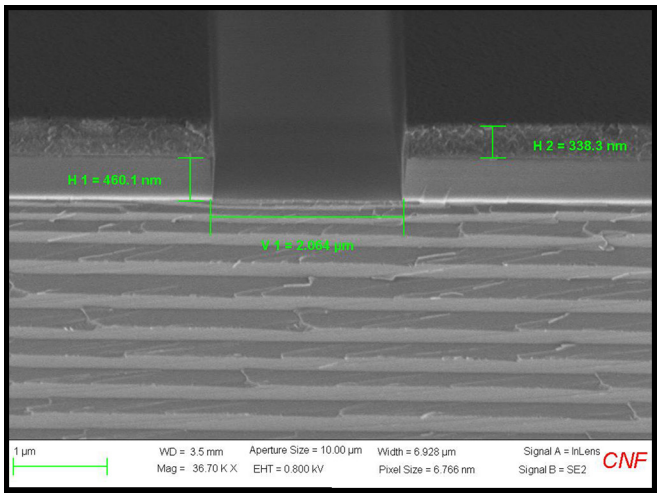


*Figure 1: 2000 nm silicon dioxide line etched with $C_3H_2F_4$ for 160 seconds. SEM image was taken at a 70-degree angle. The actual calculated thicknesses are approximately Height #1 ($SiO_2$) = 487nm and Height #2 (Photoresist)= 359 nm.*

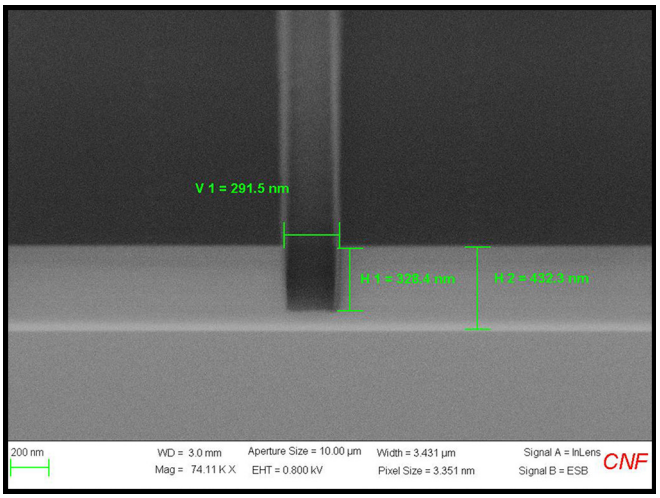


*Figure 2: 300 nm silicon dioxide line etched with $C_3H_2F_4$ for 120 seconds. The photoresist was stripped. SEM image was taken at a 70-degree angle. The actual SiO2 calculated thicknesses are approximately Height #1 = 348 nm and Height #2 = 458 nm.*

gases etched patterned wafers for two and four minutes. Feature etch rates/selectivity were determined using a KLA Tencor P-7 Stylus Profilometer by measuring an automated programed sequence of twenty step heights across the wafer. The three step heights measured were the height of the DUV 210 resist after the ARC etch, the step height after the dielectric etch, and the step height of the etch after the resist was stripped in an oxygen plasma using a SCE-110-RF Anatech Plasma Etcher. The selectivity was determined by the ratio between the $SiO_2$ and photoresist etched. Cross-sectional etch profiles were observed using a Zeiss Ultra scanning electron microscope (SEM).

## Results:

Four separate $C_3H_2F_4$ patterned etches between forty-five and two hundred forty seconds established consistent etch rates and etch selectivity for DUV 210 resist (Table 1). When compared to the two legacy gases (Table 2), $C_3H_2F_4$ had the highest etch rate for $SiO_2$. The desired selectivity between the oxide and the resist was much higher than etches using trifluoromethane and difluoromethane. Cross-sections of all $C_3H_2F_4$ patterned $SiO_2$ etches appear to have smooth, vertical sidewalls, without signs of resist undercutting (Figure 1). There was evidence of RIE lag for the narrower features (Figure 2). Overall, these etch tests demonstrated that $C_3H_2F_4$ is a viable alternative for reactive ion etching $SiO_2$.

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