Imaging Pulse-Induced Charge Density Wave Switching in 1T-TaS_2

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Primary CNF Tools Used: Zeiss Supra SEM, Nabity System for Supra SEM, CHA Evaporator, Harrick Plasma Generator

Abstract:

Charge density wave (CDW) is a macroscopic quantum state observed in low-dimensional materials, such as the two-dimensional (2D) layered material tantalum disulfide (TaS_2). In the 1T polytype of TaS_2, voltage pulses can induce CDW phase transitions, which are accompanied by a sharp insulator-to-metal transition. This makes 1T-TaS_2 promising for next-generation devices. We fabricated nanodevices of 1T-TaS_2 flakes and operated them within a scanning transmission electron microscope (STEM), allowing us to directly visualize the CDW structure and phase transitions during device operation with nanoscale spatial resolution and microsecond temporal resolution at cryogenic temperatures. Our study reveals that Joule heating drives the pulse-induced CDW transitions and the CDW transitions are directly correlated with the real-space structure and electronic properties of the material, which is crucial for developing reliable and scalable TaS_2-based electronics.

Summary of Research:

Charge density waves (CDWs) are periodic modulations of the electronic charge density within a material, which are accompanied by periodic distortions in the material's crystal lattice [1]. 1T-TaS_2 is a 2D quantum material that hosts several distinct CDW phases [2]. These include an insulating commensurate (C) CDW phase with long-range order, a metallic nearly-commensurate (NC) phase characterized by domains of commensurate CDW separated by phase slips (discommensurations), and a metallic incommensurate (IC) CDW phase lacking long-range order [3]. Below 200 K, 1T-TaS_2 is in the insulating C-CDW phase, but voltage pulses can switch it to the metallic NC-CDW phase [4]. This switching is fast, reversible and energy efficient, and results in a large change in electrical resistance, making 1T-TaS_2 promising for use in memristive and neuromorphic devices [5]. However, the mechanism of pulse-induced switching is not fully understood. To use TaS_2 in nanoscale devices, it is crucial to have a detailed understanding of how the CDW phase transitions occur at nanoscale dimensions, and what factors affect the transition.

We fabricated 2-terminal devices by exfoliating ~ 55 nm thick flakes of 1T-TaS_2 from bulk crystals onto *in-situ* TEM chips. Electrical connections to the platinum electrodes on the *in-situ* TEM chips were made by placing graphite electrodes on the TaS_2 flakes (Figure 1a,b). We operated this device within a TEM using a Keithley 2400 source meter to measure the resistance of the flake as a function of temperature. Simultaneously, electron diffraction was acquired to measure the domain size (D_{NC}), the order parameter for the C to NC transition in 1T-TaS_2, hence characterizing its CDW state (Figure 1c) [6]. In the C-CDW phase, D_{NC} is > 100 nm while in the NC-CDW phase, D_{NC} is ~ 10 nm (Figure 1).

By applying a constant DC bias and heating the flake from the C to NC phase, we monitored the device resistance and D_{NC} (Figure 1c,d). We found that the domain size changes first, followed by the resistance change, showing that the structural CDW transition precedes the resistive transition by about 10 K, as indicated by changes in resistance and domain size during the C to NC transition (inset Figure 1d). This is unexpected, as the structural and electronic changes due to CDW transitions are assumed simultaneous.

To investigate this further, we applied a series of short square pulses with increasing voltage amplitudes (2 V to 9.6 V, 3 μs pulse duration; Figure 2) to the TaS_2 flake in its C-CDW phase, using a Keysight 33600A waveform generator. For voltage pulses > 3.2 V, the flake transitions to the NC phase (Figure 2). Consistent with our earlier findings the structural CDW transition

preceded the electronic resistance transition. Additionally, larger voltage pulses produced smaller CDW domains and lower device resistance in the NC phase, suggesting that the applied voltage increases the temperature of the device through Joule heating.

To demonstrate that Joule heating drives the switching, we applied triangular voltage ramps (with maximum voltage between 0.1 V to 1.2 V) while collecting diffraction patterns at every 10 ms interval. We observed that voltages above 0.8 V caused a sudden decrease in DNC, indicating a transition from the C to NC and IC phases (Figure 3a). We extracted the in-plane flake strain from the diffraction data and converted it to corresponding temperature using thermal expansion coefficient.

At the 0.8 V threshold, we measure the flake temperature to be ~200 K, which corresponds to the C to NC transition temperature (Figure 3b). Thus, Joule heating from the applied voltage is sufficient to raise the temperature of 1T-TaS_2 devices above the CDW transition temperature.

Conclusions and Future Steps:

Our study conclusively demonstrates that bias-induced switching in 1T-TaS_2 is driven by Joule heating, causing a rapid thermal transition from the C to NC and IC phases. This mechanism applies for both steady-state biasing and microsecond voltage pulses. Further work is needed to study the claims of picosecond switching with energies below the Joule heating threshold, to determine if purely field-induced switching is possible. Our findings provide a microscopic understanding of CDW behavior in TaS_2 devices and provide a foundation for future studies to enhance the performance and reliability of TaS_2-based electronic devices.

References:

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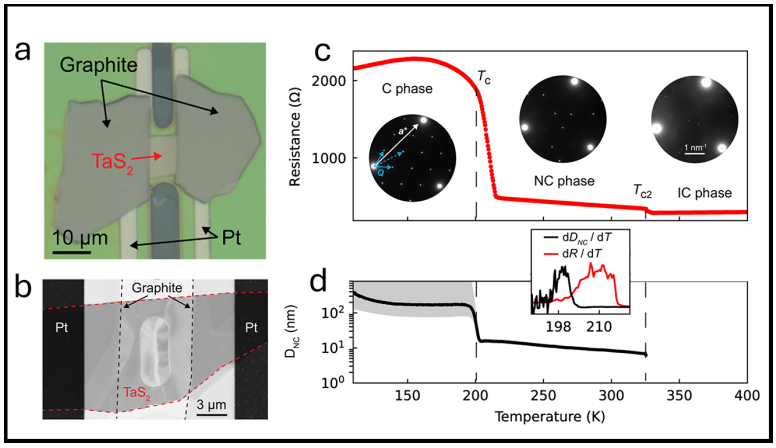

Figure 1: a. Optical microscope image of the studied device. b. STEM image of the same device. c. Resistance vs. temperature of the TaS_2 device measured in-situ *inside the TEM. Insets show associated electron diffraction pattern for each phase. d. Doman size (D_{NC}) as a function of temperature. The inset shows the temperature derivatives of the resistance and D_{NC}.*

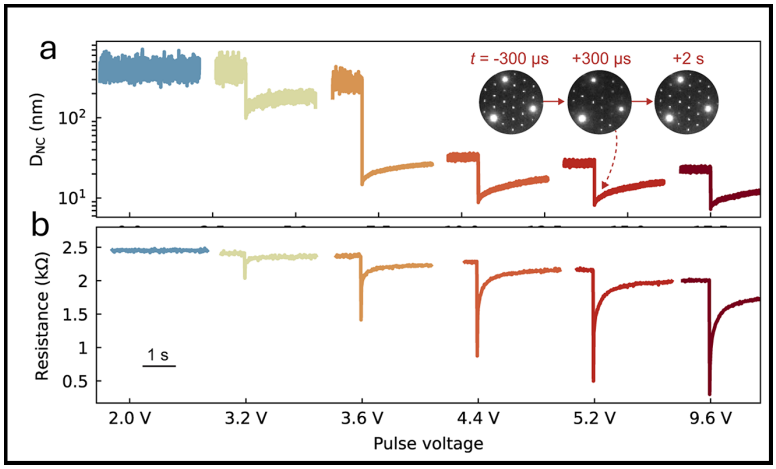

Figure 2: a. Time-resolved CDW domain size D_{NC}, and b. device resistance during pulsing.

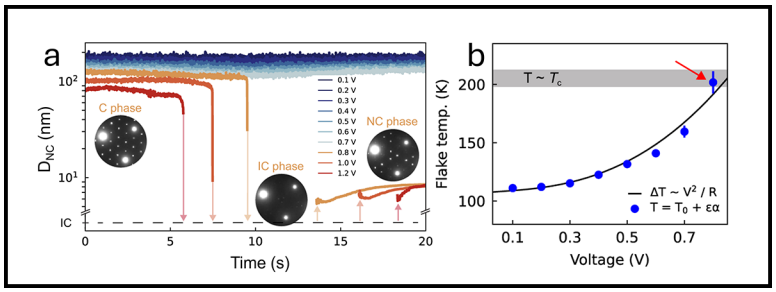

Figure 3: a. Measured D_{NC} during voltage ramps, with maximum voltage ranging from 0.1 V to 1.2 V. Insets show the diffraction pattern snapshots acquired during the 0.8 V ramp. b. Maximum flake temperature for voltage ramps from 0.1 V to 0.8 V.