Quasi-2D Materials for Ultra-Low Resistance Electrical Interconnects

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Primary CNF Tools Used: General Materials Anneal Furnace, Veeco Savannah ALD, Woollam RC2 Spectroscopic Ellipsometer, AJA Sputter Deposition, ABM Contact Aligner, GCA AutoStep 200 DSW i-Line Wafer Stepper, Heidelberg Mask Writer, YES Vapor Prime Oven, AJA Ion Mill, Glen 1000 Resist Strip, Dektak XT Profilometer, Zeiss Ultra SEM

Abstract:

The dramatic increase in the resistivity of interconnect lines with decreasing dimensions presents a significant bottleneck for further downscaling of integrated circuits [1]. This is because current interconnects use 3-dimensional metals that experience increased interface electron scattering as the interconnect dimensions approach their electron mean free path. A possible solution is to use metals with much lower electron mean free paths such as: W, Mo, and Ru. Metallic delafossite oxides are an alternative solution because of their inherent advantages over traditional metals such as: ultra-low room temperature resistivity, potential mitigation of interface/surface scattering due to their 2D Fermi surface, potentially decreased likelihood of electromigration, and potentially better compatibility with low-K oxide dielectrics. Metallic delafossite can prove to be a disruptive new material for ultra-scaled electrical interconnects.



Figure 1: Layered crystal structure of delafossite PtCoO2.

Delafossites are layered oxides with the formula ABO2 where A is a metal cation that forms 2D sheets separated by the BO2 transition-metal oxide octahedra, Figure 1. In this study we focus on metallic delafossites PtCoO2 and PdCoO2 because of their ultra-low room temperature resistivity of 2.1 $\mu\Omega$.cm and 2.6 $\mu\Omega$.cm, respectively, which is comparable to the current semiconductor industry standard interconnect metal, Cu, Figure 2 [2]. The metallic delafossite structure has an anisotropic nature with resistivity along the c-axis a factor of 500 higher than resistivity within the Pt/Pd sheet. Due to the layered crystal structure, the Fermi surface of the metallic delafossites is cylindrical as for a 2D metal. This quasi-2D crystal structure can potentially mitigate interface and surface scattering since the electron Fermi velocity does not have components perpendicular to the Pd/Pt sheets. This can potentially overcome the resistivity penalty encountered by conventional 3D metals in ultrathin films (< 20 nm). Additionally, the unique Fermi surface topology allows for an electronphonon coupling constant that is a factor of 3 lower than copper [3].

Our focus has been to demonstrate metallic delafossites as a disruptive new material for ultra-scaled electrical interconnects, for which we have two goals. The first goal is to realize their unique electrical properties and the second goal is to demonstrate the growth of highly quality delafossite thin films via atomic layer deposition (ALD) a back-end-of-the-line (BEOL) compatible synthesis technique.

Summary of Research:

To realize the unique electrical properties of delafossite thin films we have been investigating the structural and electrical properties of PdCoO2 thin films grown via molecular beam epitaxy (MBE). MBE has been shown to achieve highly crystalline films which is critical for electrical property characterization due to the structure-property relation [4,5]. We used high-resolution X-Ray diffraction (HRXRD) to confirm that the films are phase-pure. We measured the resistivity of the films using a van der Pauw geometry and modelled the resistivity scaling with film thickness using Fuchs-Sondheimer (FS) and Mayadas-Shatzkes (MS) model. The upshot being that a 50 nm thick PdCoO2 film has a resistivity of ~8 μ Ω.cm. It should be noted that while our XRD phi scans did reveal in-plane twinning our resistivity fitting did not find twin boundaries to be a significant contributor to resistivity.

In addition to modeling the resistivity scaling with thickness, we are also modeling the line-width resistivity scaling into the sub 100 nanometer regime. Towards this we have fabricated micron wide wires via the contact aligner and are fabricating sub-micron wires via the i-line stepper. It is important to scale down incrementally so to check for any lithography-related degradation of the delafossite wires which would make it difficult to isolate the dimension dependent resistivity change.

We are also investigating back-end-of-the-line (BEOL) compatible growth of these materials via Atomic Layer Deposition (ALD) and Sputtering. To guide this effort we have created a thermodynamic model of the PdCoO2 system and are validating it via ex-situ anneals in relevant ambients, temperatures, and time scales to find BEOL conditions in which these materials are stable.

Conclusions and Future Steps:

We have three main goals: (1) Characterize the line-width resistivity scaling of these delafossite materials, (2) map out their stability in BEOL conditions, and (3) find a BEOL compatible growth method.

References:

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Figure 2: Comparison of room temperature resistivity of PdCoO, and PtCoO, to conventional interconnect metals.