ASIC Design for a Fast X-Ray Pixel Array Detector

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Primary CNF Tools Used: Cadence Virtuoso Software

Abstract:

The first Keck X-ray pixel array detector (Keck-PAD) was developed at Cornell University in the late 2000s. It is a high speed, high flux, photon burst detector that can take and store eight images at an image rate of roughly 10 MHz. It was designed to study fast condensed matter physics processes, such as crack propagation and materials failure, via x-ray diffraction at synchrotron storage ring x-ray sources, such as the Cornell High Energy Synchrotron Source (CHESS). However, synchrotron sources continue to advance in speed and brilliance thereby opening opportunities to study processes that require imaging at rates that exceed 10 MHz. Methods to create the K3 test chip (K3TC) — a chip with faster pixel electronics that follows in the footsteps of the original Keck detector — are presented in this report.

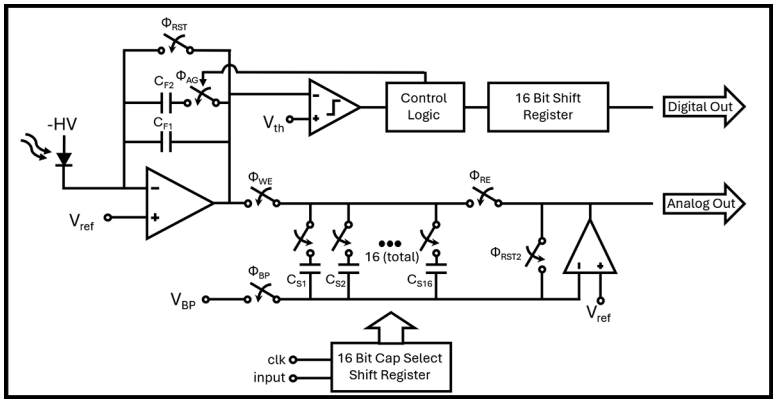

Figure 1: Block diagram of a single pixel for the K3TC.

Summary of Research:

The K3TC ASIC is organized as a 16 x 16 imaging array. A block diagram of the K3TC pixel can be seen in Figure 1. Incoming X-rays strike a semiconductor sensor, represented with a reverse biased diode in the diagram. This creates a correlated number of electron-hole pairs that are then separated by a large high voltage bias. K3TC can collect either electrons or holes, depending on the sensor. Once the charge has been collected, it is then integrated across CF1. A corresponding voltage is then produced at the output node of the amplifier. If this output voltage crosses an externally set threshold, VTH, then the pixel triggers adaptive gain, closing .AG, and adding more capacitance to the integrator. This, in turn, decreases the gain of the integrator, allowing it to collect more X-rays before saturating. At the end of an image the voltage is stored on a storage capacitor (CS1, CS2, etc.) and if the adaptive gain has been triggered, a digital "1" is added to the 16-bit shift register. The front end is then reset via .RST, and the next storage capacitor is switched in. The process is then repeated until all sixteen images have been taken.

After all sixteen images have been collected, the data is read off chip at a much slower rate. The analog and digital data is streamed from the chip in different channels and the analog data is converted to digital off chip. It is then passed into an FPGA, processed, and passed into a computer.

The first step of the current project was to identify the pain points in the previous Keck PAD. Real world tests found that the original Keck PAD could run at about 10 MHz (100ns per frame), but image quality began to break down at higher speeds [1]. Simulations performed in Cadence Virtuoso were used to identify limitations in the front-end amplifier and the reset switch. As can be seen in Figure 1, the design relies on an integrating op-amp, which needs to be fast to allow for the detector to keep up with all the large amount of signal. A new amplifier was drafted and simulated. It sacrifices DC gain for speed, while maintaining similar amounts of power draw. A new simple redesign of the reset switch reduced the on resistance, which speeds up resets.

Next, elements from another ASIC designed in the group, the Mixed-Mode PAD (MM-PAD) — a continuous imager designed for longer time scale, higher flux experiments than K3TC [2] — were incorporated and a K3TC test chip was submitted and fabricated in TSMCs 180 nm node size.

Conclusions and Next Steps:

A first step towards a fast X-ray pixel array detector was achieved, opening opportunities to study processes that require imaging at rates that exceed 10 MHz. A fast front-end amplifier was designed and a 16 x 16 pixel ASIC was fabricated in TSMC's 180 nm node size. Next, the functionality of the ASIC will be tested. For this purpose, a PCB has been developed to hold, power, and control parts of the chip. Data processing and finely tuned digital control will be done on an FPGA. Tests will focus primarily on speed, as well as noise performance, power consumption, and readout. Multiple test structures have been built into the chip and will be used to verify functionality of its components. Additionally, X-ray sensors will be bonded to the ASIC and tests will be conducted using optical pulsed lasers and X-rays sources.

References:

[1] L. Koerner, "X-ray analog pixel array detector for single synchrotron bunch time-resolved imaging," Cornell University, 2010.

[2] K. S. Shanks, Characterization of a Small-Scale Prototype Detector with Wide Dynamic Range for Time-Resolved High-Energy X-Ray Applications, Cornell University: IEEE, 2021.