

System-on-Foil

CNF Project Number: 3028-22

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*Primary CNF Tools Used: Electron-beam Evaporator (Odd & Even Hour), AJA Sputter, PT740,
Trion III Minilock, SEM Supra & Ultra, Logitech CMP Orbis, Oxford PECVD,
Heidelberg Mask Writer DWL2000, DISCO Dicing Saw, Oxford FlexAL, Savannah ALD*

Abstract:

Lux Semiconductors is developing a new system-level advanced packaging technology, System-on-Foil, designed to overcome limitations of current packaging technologies. This architecture integrates a patterned metal core substrate, facilitating high-speed signal transmission between redistribution layers on the top and backside. Copper transmission lines are patterned in silicon wafer toolsets to achieve interposer-like densities, enabling high bandwidth, low latency routing for chiplet-based heterogeneous integration. The rigid metal substrate allows for thicker dielectric layers that enable low loss high speed transmission lines, leveraging the metal substrate as reference ground. High speed signal can be routed through the metal core in impedance matched coaxial vias with near zero crosstalk. The metal core also provides good thermal conductivity, CTE compatibility with silicon, and durability even in ultra-thin form factors.

Summary of Research:

Layers of circuitry containing oxides and metals are deposited and processed onto thin, metal wafers to

realize interposer chiplets with 2.5D architecture. These chiplets act as intermediaries in the signal routing and delivery between transistor and PCB domains.

Conclusions and Future Steps:

We have realized thin, metal foil interposers, and integrated them with traditional and flexible hybrid electronics to demonstrate our technology. Our more recent work has been focused on increasing the number of layers with applications toward integrating high bandwidth memory with compute modules, photonics, and nurturing the chiplet ecosystem. Our future steps are to continue to deliver on our customer's needs. At the CNF, we look to learn and adapt to the challenges that are associated with layering thick oxides and metals together to achieve several-micron tall layer stacks. Development of our platform is also taking place at other NNCI institutions, such as Georgia Tech and U Penn.

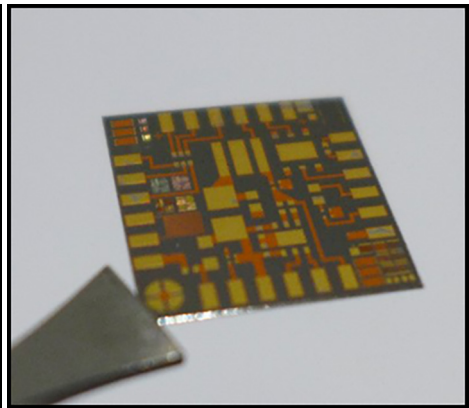
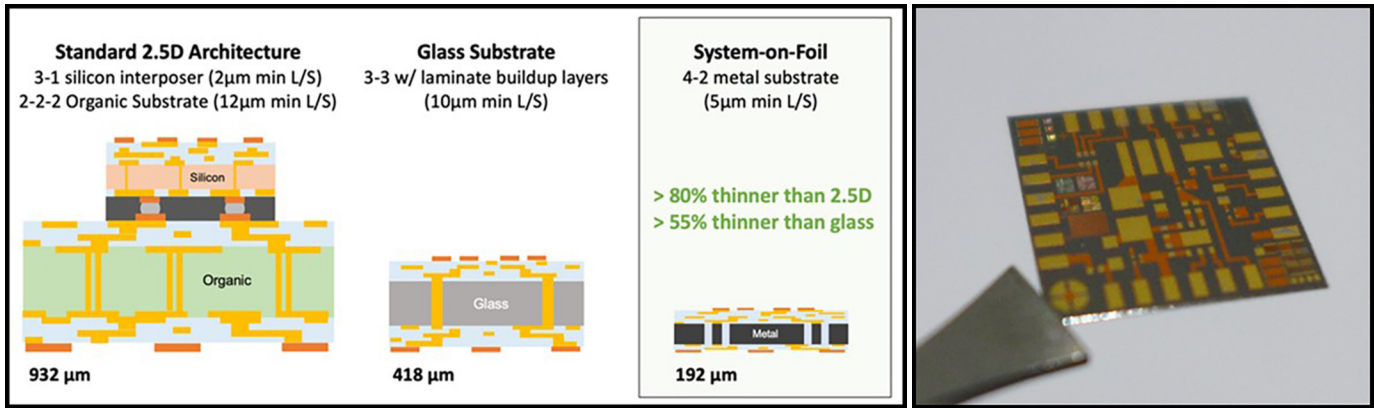


Figure 1: Advanced packaging cross sectional comparison.

Figure 2: Completed metal foil interposer.

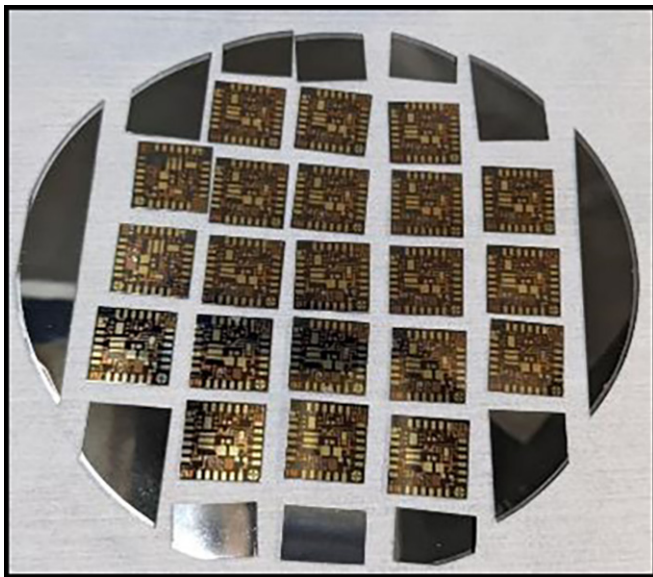


Figure 3: Completed 100 mm diameter metal foil substrate containing 21 interposers.

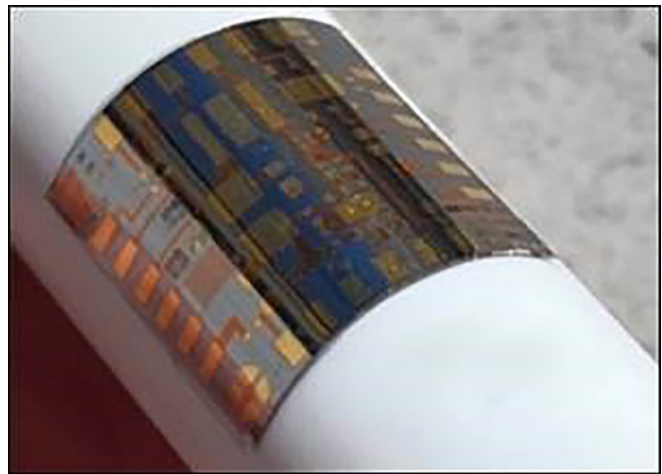


Figure 4: Metal foil interposer wrapped around a tube of Chapstick.