Ferroelectric Hafnium Zirconium Oxide Under the Gate of AlN/GaN High Electron Mobility Transistors

CNF Project Number: 2801-19
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Primary CNF Tools Used: GCA AutoStep 200 DSW i-line Wafer Stepper, SC4500 Odd-Hour Evaporator, PT770 Etcher, Rapid Thermal Anneal - AG Associates Model 610, Arradiance ALD Gemstar-6, JEOL JBX-6300FS

Abstract:

Gallium nitride-based high electron mobility transistors (GaN HEMTs) are at the cutting edge of technological innovation. Renowned for their high speed and power capabilities, GaN HEMTs are utilized across a diverse array of sectors, including telecommunications, power electronics, aerospace, defense, industrial, medical, and consumer electronics. Integrating GaN with an aluminum nitride (AlN) barrier enhances speed, power output, and thermal management. However, traditional HEMTs are reaching their physical limits. The work in the CNF investigates the addition of a ferroelectric hafnium zirconium oxide (HZO) layer beneath the gate of AlN/GaN HEMTs to overcome these limitations. This is achieved through the use of the remnant polarization of ferroelectrics to modulate the threshold voltage and demonstrate the ability for memory, giving GaN HEMTs improved device performance and more functionality. Through the development of multiple HEMT devices with varying HZO thicknesses, hysteresis in device output currents is verified and alterable, with preliminary results exhibiting a threshold voltage tuning range of 0.5-1.2 V. Overall, the work lays the foundation for the benefits of incorporating ferroelectric layers under the gate of AlN/GaN HEMTs.

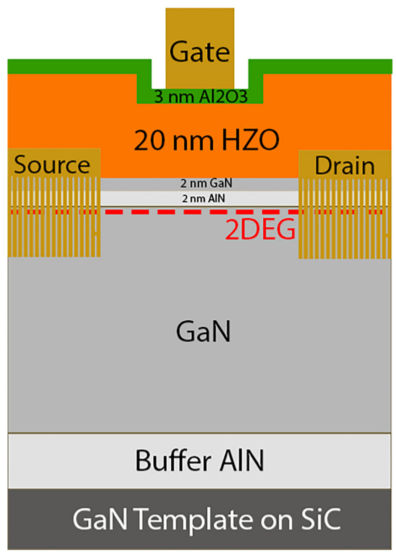


Figure 1: Schematic image of processed HEMT device with alloyed contacts and an HZO layer.

Summary of Research:

As the demand for higher performance devices grows and transistors continue to scale down, discovering new materials to enhance device performance or introduce new functionalities becomes increasingly critical. One promising approach is integrating a ferroelectric layer beneath the gate of High Electron Mobility Transistors (HEMTs). When combined with the polarization-induced two-dimensional electron gas (2DEG) of an AlN/GaN heterostructure, the ferroelectric layer's ability to switch polarization can modify the device's threshold voltage. This modification is achieved through ferroelectric polarization, which alters the polarization at the heterostructure interface.

To demonstrate this feature, HEMT devices were fabricated at the CNF. Figure 1 presents a schematic of the processed device. The fabrication process involves the following steps: (1) device isolation, (2) ohmic contact metallization, (3) HZO deposition, (4) annealing, and (5) gate metallization. Steps 1, 2, and 4 employ the GCA AutoStep 200 DSW i-line Wafer Stepper to define optical patterns for subsequent steps. Additionally, Step 4 uses the JEOL JBX-6300FS for defining electron beam lithography (EBL) gates. Device isolation is performed via etching in the PT770 Etcher, while ohmic and gate metallizations are conducted in the SC4500 Odd-Hour Evaporator. HZO and Al2O3 layers are deposited using the Arradiance ALD Gemstar-6 and annealed in the

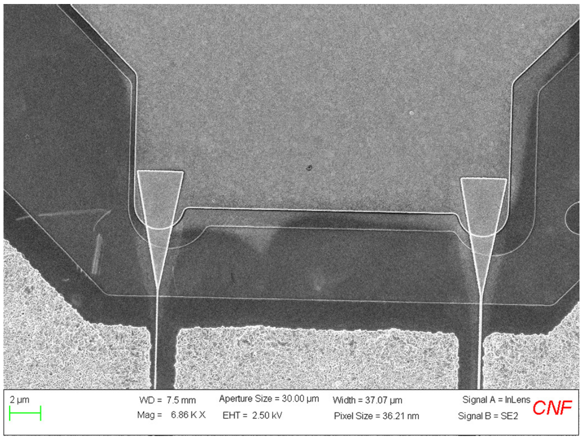
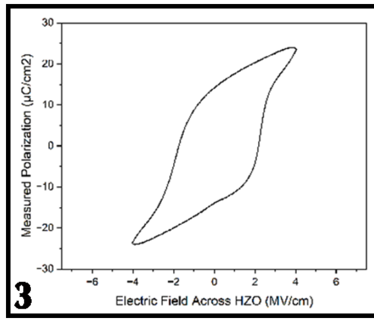


Figure 2: SEM of EBL deposited gate.



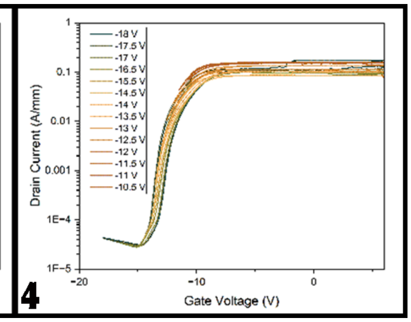


Figure 3, left: P-E loop of the deposited HZO layer in a metal-ferroelectric-metal structure.

Figure 4, right: Transfer Curve of HEMT device with HZO at multiple gate voltage sweeps, demonstrating threshold voltage modulation.

Rapid Thermal Anneal - AG Associates Model 610. Figure 2 shows scanning electron microscope (SEM) images of the deposited EBL gates between the source and drain contacts.

The ferroelectric properties of the HZO layer can be evaluated using a polarization-electric field (P-E) loop. Figure 3 illustrates the P-E loop of the deposited HZO layer. The remnant polarization of the HZO films was measured at 14.155 .C/cm., which is slightly lower than the typical values reported in the literature (~17 .C/cm.).

Due to the ferroelectric properties, the drain current versus gate voltage graphs display a counterclockwise hysteresis loop during dual sweeping of the gate voltage. Adjusting the sweep range of the gate voltage results in a threshold voltage modulation. Figure 4 demonstrates a 1 V threshold voltage tuning range, which is achieved by varying the gate voltage sweep ranges.

Conclusions and Future Steps:

Five different devices were fabricated, each with varying thicknesses of HZO. Through these devices, the study aimed to demonstrate the ability to modulate the threshold voltage, reduce gate leakage, and exhibit memory storage capabilities. The transfer curves of the devices exhibited distinct counterclockwise hysteresis. This hysteresis, along with the modulation of the gate voltage, demonstrated a 1 V threshold voltage tuning range, as well as indicating the memory capabilities of the device. Additionally, the gate leakage current in samples with HZO was reduced by approximately six orders of magnitude compared to those without HZO.

Given the slight decrease in the remnant polarization of the HZO layer compared to in literature, future work should focus on analyzing devices with a more robust HZO layer. This improvement could result in a larger memory window in the transfer curves and a greater threshold voltage tuning range.

In addition to perfecting the deposition of the HZO layer, exploring other ferroelectric materials could yield better interaction with the AlN/GaN heterostructure. Currently, significant research is focused on ferroelectric aluminum scandium nitride (AlScN). As AlScN is a nitride and can be deposited using Molecular Beam Epitaxy, it is possible to develop an all nitride ferroelectric HEMT heterostructure in-situ. This approach could result in cleaner interfaces, larger hysteresis curves, and improved device performance.

References:

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