Fabrication of 2D-Material-Based Ionic Transistors

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Summer Program(s): 2024 Cornell NanoScale Facility Research Experience for Undergraduates (CNF REU) Program
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Mentor(s): Kaushik Chivukula, Graduate Student, Materials Science and Engineering, Cornell University
Primary Source(s) of Research Funding: National Science Foundation under Grant No. NNCI-2025233
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Summer Program Website: https://cnf.cornell.edu/education/reu/2024
Primary CNF Tools Used: Heidelberg Mask Writer DWL-2000, ABM Contact Aligner, Oxford 81 RIE, AJA Ion Mill, SC4500 Even-Hour Evaporator

Abstract:

Traditional electronic field-effect transistors (FETs), which utilize electrons and holes as charge carriers, are indispensable in modern electronic devices such as integrated circuits and microprocessors. They form the backbone of today's digital technology by enabling efficient information processing, storage, and transmission. Despite ongoing challenges in the miniaturization of electronic transistors, ionic FETs offer distinct advantages, particularly biocompatibility and tunable conductance. Our project aims to fabricate ionic transistors using advanced 2D materials and address the limitation of low on-off current ratios in these devices.

Summary of Research:

The human brain, with its highly selective ionic transmission system, processes vast amounts of information and facilitates neural communication daily. To mimic the ultra-functional capabilities of the brain, nano-channeled ionic field-effect transistors that use ions like Na+ and Ca2+ as carriers, similar to those in neural processes, show great potential for future applications. Such transistors are promising for artificial brain systems and memory devices like neuromorphic memristors due to their unique ability to maintain discrete conductivity states, which serve as memory storage units.

In order to replicate the ultra-selectivity of brain ionic channels and increase the on-off ratio, we focused on fabricating ionic transistors with nanochannels approaching the Debye length. Conventional microchannels, characterized by their short Debye lengths and discontinuous electric field effects, often result in the undesirable coexistence of both negative and positive ions. In contrast, the nanochannel design allows the electric field to penetrate the entire channel, predominantly permitting the passage of only a single ion type. This ensures a low energy consumption in the transistor, mirroring brain functions.

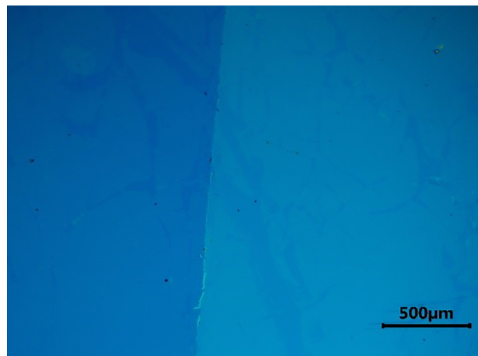
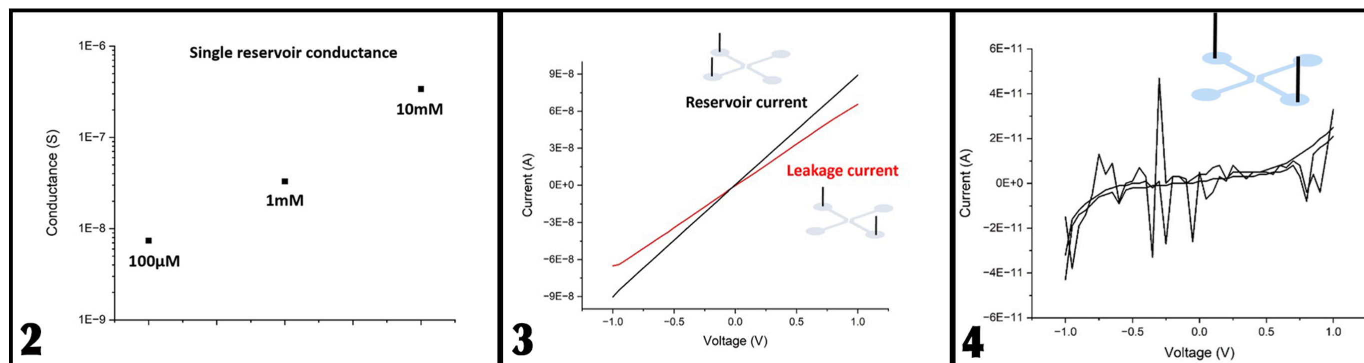


Figure 1: Stable 2D heterostructure.

We began by preparing a silicon wafer with a 300 nm thermal oxide layer, cutting it into 1-inch by 1-inch pieces. To create the nanochannel ionic pathway, we deposited a monolayer of 2D Copper-Tetrakis (4-carboxyphenyl) porphyrin (CU-TCPP) by immersing the wafer pieces in a Copper Nitrate solution, capping them with Hexane, and injecting TCPP solution using a syringe pump. After allowing the Hexane to evaporate, the remaining solution was drained. Thereafter, a monolayer of Molybdenum disulfide (MoS.) was exfoliated and transferred onto the CU-TCPP-coated pieces, resulting in the formation of a stable 2D heterostructure, as illustrated in Figure 1.

To etch the MoS. monolayer into a 100 μm by 100 μm pattern, photolithography and the AJA ion mill at the Cornell NanoScale Facility were employed. Oxygen plasma then removed the photoresist cleanly. Next, we deposited 50 nm of silicon dioxide using the Oxford Atomic Layer Deposition FlexAL machine to serve as the insulating layer of the ionic field effect transistor. The gate electrode was fabricated by depositing 10 nm of titanium and 50 nm of gold with the Thermal/E-gun Evaporation System, followed by a lift-off process using hot N-Methylpyrrolidone (NMP) stripper. The



source and drain channels were defined using SU-8 and photolithography, and subsequently etched with the Oxford reactive ion etching tool. Finally, capping the pieces with Polydimethylsiloxane (PDMS) completed the fabrication process.

For the measurement of Single Reservoir Conductance, four holes were made in the PDMS, into which sodium chloride (NaCl) electrolyte was injected. Two silver electrodes were placed in the same reservoir. With ions flowing freely within the unobstructed single fluid channel, conductivity was observed, confirming the successful fabrication of the single reservoir. Figure 2 shows the relationship between the NaCl solution concentration and its conductance, indicating that as the concentration increases, the number of ions available for carrying electric current also increases, leading to higher conductance.

During the leakage test, electrodes were placed in two separate fluid channels rather than in the same one. Without a nanochannel allowing current to flow between the channels in this case, no current should have been detected when applying voltage if there was no leakage. However, as shown in Figure 3, when voltage ranging from -1V to 1V was applied, a leakage current of approximately 10.. A was detected. This current is of the same order as that of a single connected reservoir, suggesting that some leakage was indeed occurring between the two fluid channels.

To address this issue, we applied Vapor Phase (3-Aminopropyl) triethoxysilane (APTES) treatment [1] to the PDMS to induce covalent bonding between SU-8 and PDMS, enhancing the sealing of the fluid channels.

After this optimization, we repeated the leakage test under identical conditions. This time, the current was around 10... A, which is three orders of magnitude lower than the previous leakage current, and no linear trend was observed in Figure 4. This minor current, likely due to the open holes, was close enough to zero to indicate that there was no leakage, confirming the successful fabrication of a leakage-free device, ready for future experiments and innovations.

Conclusions and Future Steps:

In conclusion, our 2D material-based ionic field effect transistors demonstrate potential for applications in future Neuromorphic Computing systems by simulating brain functions. The use of Oxygen Plasma effectively removed the photoresist, while Hot NMP facilitated the lift-off process. The leakage between source and drain channels was minimized through APTES treatment of PDMS, resulting in a non-leakage current of approximately 10... A under a voltage range of -1V to 1V. Future work should focus on testing and measuring the conductance of different organic molecule cages, which could lead to the selective manipulation of ion types passing through the transistors.

Acknowledgements:

Special thanks to the 2024 Cornell NanoScale Science & Technology Facility Research Experiences for Undergraduates (CNF REU) Program funded by the National Science Foundation under Grant No. NNCI-2025233, and the National Nanotechnology Coordinated Infrastructure. I would also like to thank Prof. Yu Zhong and Kaushik Chivukula for their mentorship, as well as the CNF staff and program coordinators for their support.

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Optimizing Annealing Temperature for Ohmic Contacts to AlGaN/GaN

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Summer Program(s): 2024 Xing Army Educational Outreach Program (AEOP), 2024 Cornell NanoScale Science & Technology Facility Research Experience for Undergraduates (CNF REU) Program

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Mentor(s): Aaron Windsor, Cornell NanoScale Facility, Cornell University; Joseph Dill, Applied Engineering Physics, Cornell University; Jimy Encomendero, Electrical and Computer Engineering, Cornell University

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Summer Program Website: https://cnf.cornell.edu/education/reu/2024

Primary CNF Tools Used: GCA AS200 i-line Stepper, Glen 1000 Resist Strip, SC4500 Odd-Hour Evaporator, Rapid Thermal Annealer (RTA), Zeiss Supra SEM, Bruker Energy-dispersive X-ray Spectrometer (EDS), Optical Microscope

Abstract:

As ultra-wide bandgap semiconductor research progresses, the need for reliable, low-resistivity ohmic contacts becomes more essential. To ensure high contact quality and reproducibility, process conditions must be carefully optimized. This project specifically analyzed the impact of various annealing temperatures on a Ta/Al/Ni/Au metal stack to minimize contact resistance. Previously, annealing at 830°C under N2 ambient showed lateral metal diffusion, known as contact spreading, leading to the transistor short-circuiting and preventing the measurement of contact resistance. GaN pieces were first coated with photoresist, onto which transfer length method patterns were transferred using the GCA AS200 i-line stepper. The SC4500 Odd-Hour evaporator was then used for e-beam evaporation of 20 nm tantalum, 50 nm aluminum, 100 nm nickel, and 40 nm gold. After liftoff, the samples were analyzed and measured under the Zeiss Supra Scanning Electron Microscope (SEM). The samples were then annealed in N2 ambient at temperatures ranging from 500, 600, 700, 800, and 900°C. Using the SEM and its Energy Dispersive Spectroscopy (EDS), the spreading of the metals was measured. Lastly, using the transfer length method, the optimal annealing conditions for the lowest contact resistance were explored.

Summary of Research:

Silicon Process and Results. The spreading under investigation was seen previously on a 20 nm tantalum, 150 nm aluminum, 50 nm nickel, and 50 nm gold stack on GaN. Thus, the process started by recreating this metal stack onto four 8 x 8 mm Si pieces in order to trial the process. First, each piece was cleaned with sonication in acetone, isopropyl alcohol, and deionized water for 5 minutes each. Then, to remove any excess moisture, the pieces were placed on a hotplate at 110°C for five minutes. From there, AZ NLOF 2020 negative photoresist was spun onto each piece, with a target width of 1.1 μm, and then they were baked at 115°C for 60 seconds. The GCA AS200 i-line stepper exposed each piece in four spots with an Ohmic contact mask. After baking these pieces again at 115°C for 60 seconds on a hotplate, they developed in 726 MIF for 60 seconds, removing the unexposed photoresist. The Glen 1000 Resist Strip removed any excess organic matter or resist on the pieces. To deposit the metal stack, the SC4500 Odd-Hour electron beam evaporator was used. Liftoff consisted of 10 minutes in Microposit Remover 1165, five minutes isopropyl alcohol, both in sonication, then a rinse with deionized water. Under the Zeiss Supra SEM, the Circular Transfer Length Method (C-TLM) spacings were measured, and EDS baseline images were taken. Then, the four pieces were annealed at 700, 750, 800, and 850°C for 60 seconds under N2 ambient in the Rapid Thermal Annealer (RTA). Again, the pieces were analyzed under the SEM with EDS to examine any spreading.

Before annealing, the circle lines were crisp, as seen in Figure 1(a). After annealing, visual spreading of aluminum could be seen under both the optical microscope and the SEM, as in Figure 1(b). Additionally, annealing induced nickel clumping. This can be seen in the EDS images in Figure 2. This effect is likely due to the high surface energy of nickel. Since aluminum melts at 660°C, it likely forms a liquid at an annealing temperature above this. Because the nickel sits atop this aluminum liquid, to reduce its surface energy, the nickel

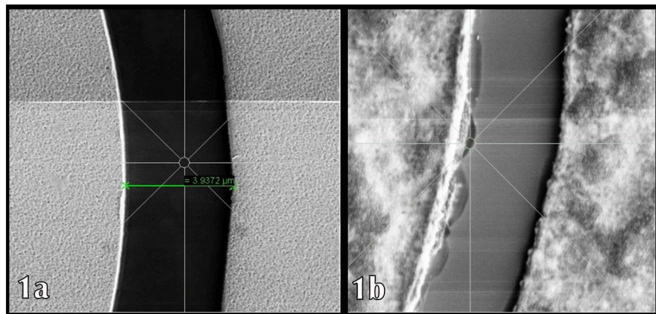

Figure 1: (a) Si Sample 2 µm Gap Pre-anneal. (b) Si Sample 2 µm Gap Annealed at 850°C.

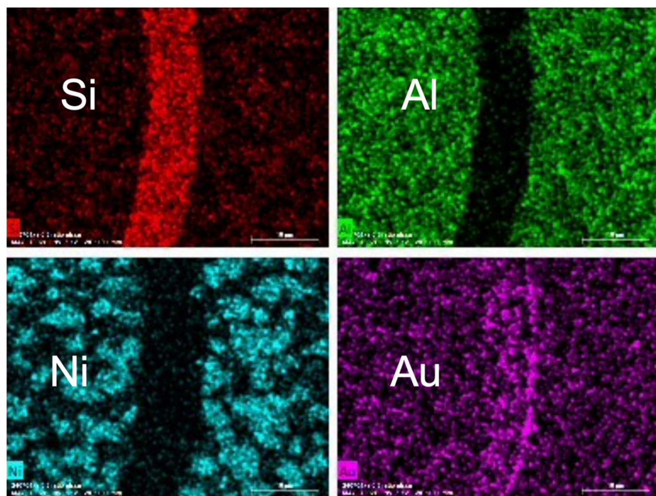

Figure 2: Si Sample 2 µm Gap Annealed at 700°C.

obtains a lower surface energy by forming spheres. This causes the clumping effect.

GaN Process and Results. The fabrication process with five 10 x 10 mm GaN pieces was identical to that of the Si pieces, except before the electron beam deposition, the pieces were cleaned in HCl, deionized water, BOE, and deionized water again for 60 seconds each. Additionally, the Ta/Al/Ni/Au metal stack was changed to 20 nm tantalum, 50 nm aluminum, 100 nm nickel, and 40 nm gold. The intention was to reduce the amount of aluminum liquid that the nickel layer sits atop to prevent the nickel clumping. Also, the thickness of nickel was doubled to encourage it to remain flat instead of clumping and forming spheres. The five GaN pieces were annealed at 500, 600, 700, 800, and 900°C, and the 800°C sample was measured on a probe station.

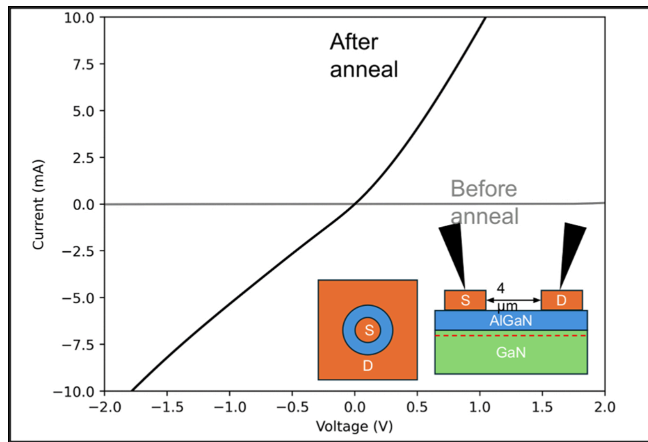

Figure 4: TLM Measurement for 800°C GaN Sample.

On GaN, there was no visual spreading as there was on the Si, but a "bubbling" effect was observed. This bubbling is evident in Figure 3(a). Figure 3(b) and 3(c) show that these bubbles are actually voids of gold and nickel, so they are different from the nickel clumps seen on Si. Annealing the GaN at 800°C increased the amount of current that could pass through the contact by roughly two orders of magnitude, as shown in Figure 4. Although, the contact is still not Ohmic, as Current vs Voltage is not linear.

Conclusion and Future Steps:

Varying the annealing temperature of the Ta/Al/Ni/Au stack on GaN from 500 to 900°C showed minimal spreading but an increasing "surface bubbling" effect as temperature increases. Nickel clumping as well as spreading on the Si pieces was evident after annealing, and future TLM measurements on the GaN pieces will determine the annealing temperature with the lowest contact resistance.

Acknowledgements:

The author would like to thank: the Army Educational Outreach Program; the Cornell NanoScale Facility Research Experiences for Undergraduates program; Professor Grace (Huili) Xing; Aaron Windsor.

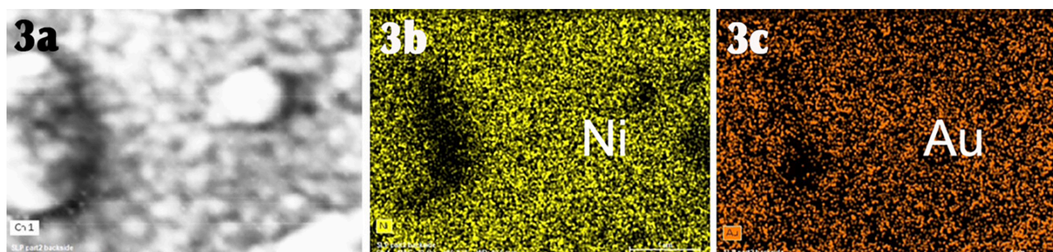

Figure 3: (a) GaN SEM. (b): Ni EDS. (c) Au EDS.

Fabrication of Interdigitated Electrodes for use in a Homebuilt Electron Force Microscope

CNF Project Number: 863-00
Principal Investigator(s): John A. Marohn
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Primary Source(s) of Research Funding: NSF Award # DMR-2113994

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Primary CNF Tools Used: Hamatech Hot Piranha Cleaner, Class II Resist Spinners, Edge Bead Removal System, ABM Contact Aligner, Hamatech Wafer Processor, SC4500 Odd-Hour Evaporator, DISCO Dicing Saw

Abstract:

Interdigitated electrodes are under development for applications in electron force microscopy. These devices will be employed in the investigation of charge recombination dynamics in organic photovoltaic devices.

Summary of Research:

The fabrication of interdigitated electrodes (IDEs) for application in the homebuilt electron force microscopes (EFMs) of the Marohn group will be facilitated by the tools provided by the Cornell NanoScale Facility (CNF). The electrodes will be made utilizing basic photolithography and thin film deposition techniques. These devices will be used in the analysis of charge recombination dynamics in organic photovoltaic (OPV) films using a novel EFM method invented in the Marohn Lab: phase kick electron force microscopy (pk-EFM) [1]. The comb-like structure of the IDEs as shown in Figure 1 will greatly enhance the sensitivity of the new method, allowing us to make measurements with space-charge limited current.

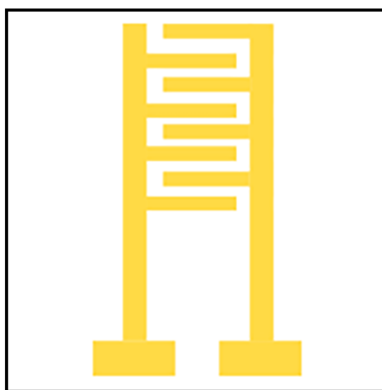

Figure 1: An Interdigitated Electrode. Interdigitated electrodes (IDEs) have a comb-like structure that increases the sensitivity of charge detection.

The process of fabricating the interdigitated electrodes will begin in photolithography room 106. Lift-off resist (LOR) will be spin-coated on a cleaned, dehydrated 100 mm quartz wafer. A soft bake will be performed at 150. by direct contact on a hot plate. Once the soft bake is complete, a compatible imaging resist will be spin-coated on top of the LOR resist and will be baked per the imaging resist's requirements. Edge beads will be removed after each spin coating step and film uniformity will be checked with the Filmetrics F50.

The IDE pattern will be written using the ABM Contact Aligner. Rachel Cohn of the Marohn Group has already written the mask for this application, so the Heidelberg Mask writers will not be utilized. Exposure conditions for this application have yet to be optimized; therefore an exposure array will be performed to determine the optimal conditions for writing the IDEs onto the stack. Once the optimal conditions have been determined, exposed stacks will be placed in the SC4500 Odd-Hour Evaporator where chromium and gold will be deposited into the pattern left behind by the mask. Microchem Remover PG will lift the resist stack and excess gold from the quartz wafer, leaving behind the gold IDEs. The devices will be removed from the wafer using the DISCO dicing saw and will be brought back to Baker Laboratory for thin film deposition. No thin film deposition onto the IDEs will be conducted in the CNF cleanroom.

Fully fabricated interdigitated electrodes will be used as substrates for the deposition of OPV materials. One particular system of interest is the known OPV blend of poly-(3-hexylthiophene) (P3HT) and [6,6] phenyl-C61-butyric acid methyl ester (PCBM), which has been studied with time-resolved microwave conductivity (TRMC) [2][3], time-resolved photoluminescence spectroscopy (TRPL) [4] and has shown to have power conversion efficiency of up to six percent when thermally annealed [5]. The added sensitivity provided by the IDEs will allow our group to better compare the experimental results of the EFM method – shown

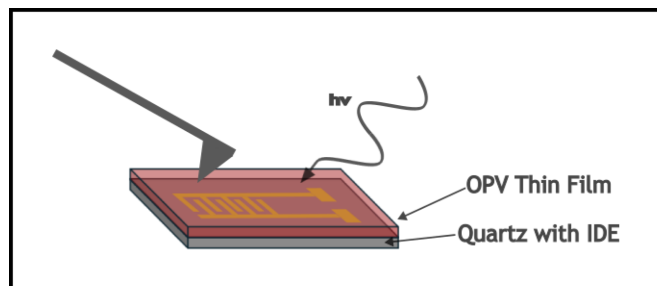

Figure 2: Schematic of Electron Force Microscope Experiment Using Interdigitated Electrodes. Interdigitated electrodes deposited on quartz substrates (bottom layer) will have an organic photovoltaic layer deposited on top of them (top layer). A conductive cantilever tip is brought close to the sample surface as it is irradiated with light. The cantilever's motion is modified by the electrostatic forces arising from the generation of charge carriers within the sample.

in Figure 2 – to those of other methods and potentially allow for the screening of promising OPV materials for incorporation into devices.

Conclusions and Future Steps:

Organic photovoltaic materials will be spin-coated on quartz substrates containing the fabricated IDEs. These samples will be inserted into Marohn Group microscopes where pk-EFM experiments will be conducted. The incorporation of the IDEs into the experiment will allow for space-charge-limited measurements of conductivity to be collected, improving the sensitivity of the experiment.

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Ferroelectric Hafnium Zirconium Oxide Under the Gate of AlN/GaN High Electron Mobility Transistors

CNF Project Number: 2801-19
Principal Investigator(s): Debdeep Jena
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Affiliation(s): Materials Science and Engineering, School of Electrical and Computer Engineering; Cornell University

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Primary CNF Tools Used: GCA AutoStep 200 DSW i-line Wafer Stepper, SC4500 Odd-Hour Evaporator, PT770 Etcher, Rapid Thermal Anneal - AG Associates Model 610, Arradiance ALD Gemstar-6, JEOL JBX-6300FS

Abstract:

Gallium nitride-based high electron mobility transistors (GaN HEMTs) are at the cutting edge of technological innovation. Renowned for their high speed and power capabilities, GaN HEMTs are utilized across a diverse array of sectors, including telecommunications, power electronics, aerospace, defense, industrial, medical, and consumer electronics. Integrating GaN with an aluminum nitride (AlN) barrier enhances speed, power output, and thermal management. However, traditional HEMTs are reaching their physical limits. The work in the CNF investigates the addition of a ferroelectric hafnium zirconium oxide (HZO) layer beneath the gate of AlN/GaN HEMTs to overcome these limitations. This is achieved through the use of the remnant polarization of ferroelectrics to modulate the threshold voltage and demonstrate the ability for memory, giving GaN HEMTs improved device performance and more functionality. Through the development of multiple HEMT devices with varying HZO thicknesses, hysteresis in device output currents is verified and alterable, with preliminary results exhibiting a threshold voltage tuning range of 0.5-1.2 V. Overall, the work lays the foundation for the benefits of incorporating ferroelectric layers under the gate of AlN/GaN HEMTs.

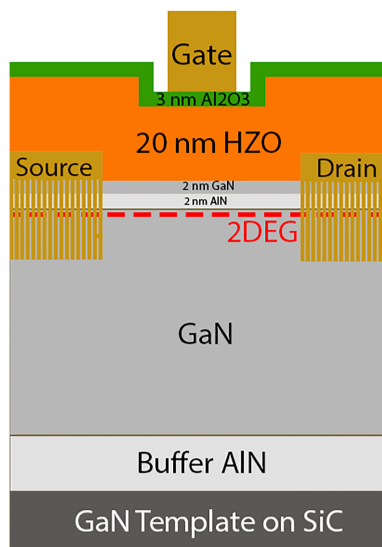

Figure 1: Schematic image of processed HEMT device with alloyed contacts and an HZO layer.

Summary of Research:

As the demand for higher performance devices grows and transistors continue to scale down, discovering new materials to enhance device performance or introduce new functionalities becomes increasingly critical. One promising approach is integrating a ferroelectric layer beneath the gate of High Electron Mobility Transistors (HEMTs). When combined with the polarization-induced two-dimensional electron gas (2DEG) of an AlN/GaN heterostructure, the ferroelectric layer's ability to switch polarization can modify the device's threshold voltage. This modification is achieved through ferroelectric polarization, which alters the polarization at the heterostructure interface.

To demonstrate this feature, HEMT devices were fabricated at the CNF. Figure 1 presents a schematic of the processed device. The fabrication process involves the following steps: (1) device isolation, (2) ohmic contact metallization, (3) HZO deposition, (4) annealing, and (5) gate metallization. Steps 1, 2, and 4 employ the GCA AutoStep 200 DSW i-line Wafer Stepper to define optical patterns for subsequent steps. Additionally, Step 4 uses the JEOL JBX-6300FS for defining electron beam lithography (EBL) gates. Device isolation is performed via etching in the PT770 Etcher, while ohmic and gate metallizations are conducted in the SC4500 Odd-Hour Evaporator. HZO and Al2O3 layers are deposited using the Arradiance ALD Gemstar-6 and annealed in the

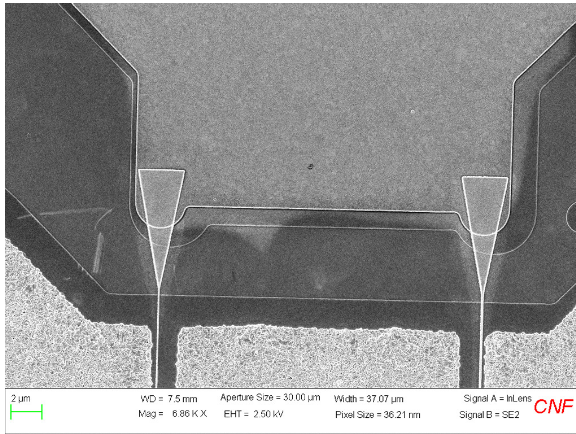

Figure 2: SEM of EBL deposited gate.

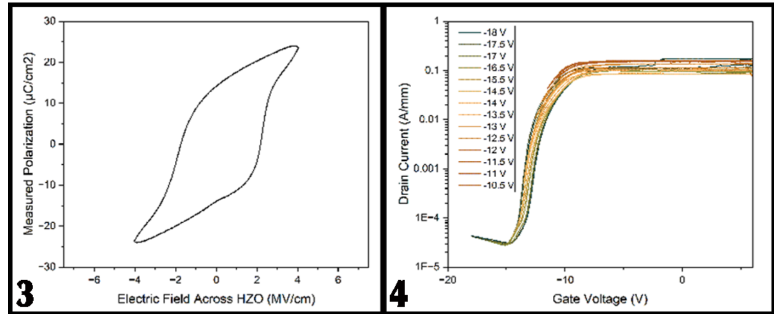

Figure 3, left: P-E loop of the deposited HZO layer in a metal-ferroelectric-metal structure.

Figure 4, right: Transfer Curve of HEMT device with HZO at multiple gate voltage sweeps, demonstrating threshold voltage modulation.

Rapid Thermal Anneal - AG Associates Model 610. Figure 2 shows scanning electron microscope (SEM) images of the deposited EBL gates between the source and drain contacts.

The ferroelectric properties of the HZO layer can be evaluated using a polarization-electric field (P-E) loop. Figure 3 illustrates the P-E loop of the deposited HZO layer. The remnant polarization of the HZO films was measured at 14.155 .C/cm., which is slightly lower than the typical values reported in the literature (~17 .C/cm.).

Due to the ferroelectric properties, the drain current versus gate voltage graphs display a counterclockwise hysteresis loop during dual sweeping of the gate voltage. Adjusting the sweep range of the gate voltage results in a threshold voltage modulation. Figure 4 demonstrates a 1 V threshold voltage tuning range, which is achieved by varying the gate voltage sweep ranges.

Conclusions and Future Steps:

Five different devices were fabricated, each with varying thicknesses of HZO. Through these devices, the study aimed to demonstrate the ability to modulate the threshold voltage, reduce gate leakage, and exhibit memory storage capabilities. The transfer curves of the devices exhibited distinct counterclockwise hysteresis. This hysteresis, along with the modulation of the gate voltage, demonstrated a 1 V threshold voltage tuning range, as well as indicating the memory capabilities of the device. Additionally, the gate leakage current in samples with HZO was reduced by approximately six orders of magnitude compared to those without HZO.

Given the slight decrease in the remnant polarization of the HZO layer compared to in literature, future work should focus on analyzing devices with a more robust HZO layer. This improvement could result in a larger memory window in the transfer curves and a greater threshold voltage tuning range.

In addition to perfecting the deposition of the HZO layer, exploring other ferroelectric materials could yield better interaction with the AlN/GaN heterostructure. Currently, significant research is focused on ferroelectric aluminum scandium nitride (AlScN). As AlScN is a nitride and can be deposited using Molecular Beam Epitaxy, it is possible to develop an all nitride ferroelectric HEMT heterostructure in-situ. This approach could result in cleaner interfaces, larger hysteresis curves, and improved device performance.

References:

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Improving Interface Quality and Repeatability in Contacts to ß-Ga2O3 by Metal-First Processing

CNF Project Number: 2802-19
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User(s): Kathleen Smith[2]

Affiliation(s): 1. School of Electrical and Computer Engineering, 2. Department of Applied and Engineering Physics; Cornell University

Primary Source(s) of Research Funding: Air Force Office of Scientific Research (AFOSR), Semiconductor Research Corporation (SRC), Defense Advanced Research Projects Agency (DARPA)

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Primary CNF Tools Used: SC4500 Odd-Hour E-Beam Evaporator, Angstrom E-Beam Evaporator, ABM Contact Aligner, AS200 i-Line Stepper, AJA Ion Mill, Glenn 1000 Resist Strip, PT720/740, PT770, RTA AG610

Abstract:

A metal-first process for forming contacts to β-Ga_2O_3 is developed that demonstrates improved contact repeatability compared to conventional liftoff processing by minimizing surface modification and results in non-alloyed contact resistances as low as 70 mΩ-mm. The metal-first process is further applied to a range of ohmic and Schottky metals with varied work functions to demonstrate that metal-first processing results in a high-quality interface that at least partially alleviates Fermi-level pinning in contacts to β-Ga_2O_3.

Summary of Research:

β-Ga_2O_3 is an ultra-wide bandgap semiconductor (~4.8 eV) with a high critical electric field, wide range of demonstrated, controllable n-type doping, sufficient electron mobility, and low-cost, native substrates that makes it potentially suitable for kilovolt device applications. Metal-semiconductor interfaces in Ga_2O_3 devices, however, are complex and inconsistent: in Schottky contacts, the Fermi-level is dramatically pinned (ie. the Schottky barrier height Φ_B does not trend linearly with the metal work function Φ_M) and measures of Φ_B can vary by over 1 eV for the same contact metal [1]. Similar variation of contact quality is observed in ohmic contacts.

The contacts reported here are formed by a metal-first process, in which the contact metal is blanket-deposited on the as-grown semiconductor surface, then patterned with photoresist (Figure 1a). The metal between the contact pads is then removed by wet and/or dry etching. This contrasts with conventional liftoff processing, where the contact area is first exposed to photoresist during patterning, then metal is deposited and the excess metal between the pads is lifted off in solvent (Figure 1b).

We fabricated both metal-first and lifted-off Ti/Au (10/110 nm) transfer length method (TLM) patterns on n+ (> 5×10^{19} cm^{-3}) Si-doped (010) β-Ga_2O_3 by electron-beam evaporation. For the metal-first contacts, TLM measurements have linear-ohmic IV behavior with a contact resistance (Rc) of 0.73 Ω-mm.

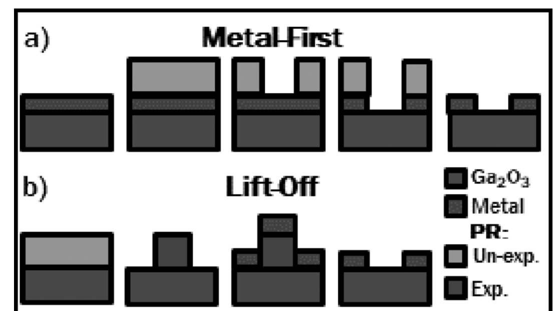

Figure 1: Process flow schematic for a) metal-first and b) liftoff contact processing.

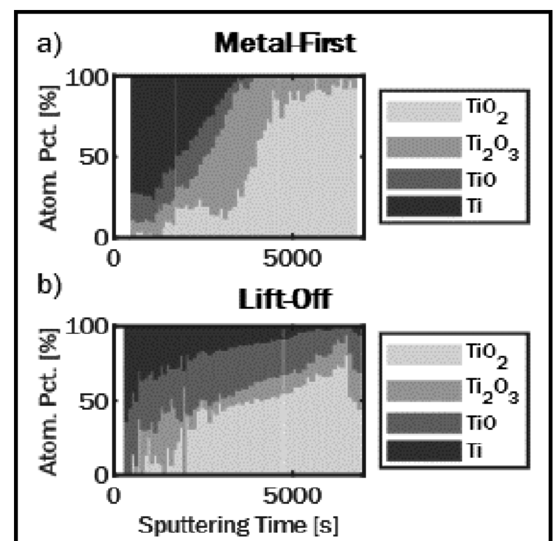

Figure 2: Comparison of Ti oxidation state from depth-resolved XPS for a) metal-first and b) lifted off Ti/Au ohmic contacts. For the metal-first contacts, Ti is fully oxidized to Ti4+ near the Ga_2O_3 interface, while for the lifted-off contacts, Ti is only partially oxidized.

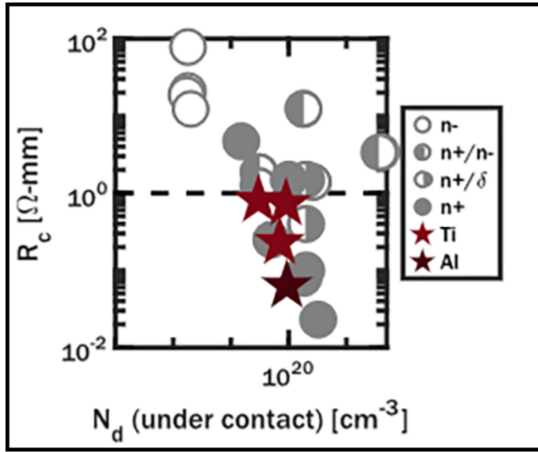

Figure 3: Bench-marking of ohmic contacts to Ga_2O_3 from literature (grey) and this work (red). The non-alloyed metal-first contacts are highly competitive with existing reports.

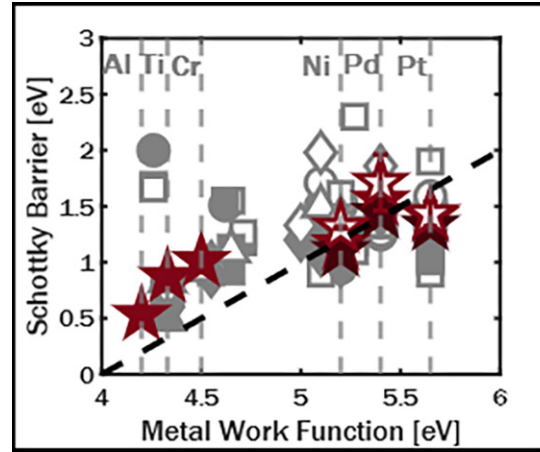

Figure 4: Measured Φ_B vs. Φ_M for contacts to Ga2O3 from literature (grey) and this work (red). The extracted Φ_B in this work increases with increasing Φ_M with a slope of 0.46 and R2 of 0.986, while reports from literature show significant Fermi-level pinning with very little dependence of Φ_B on Φ_M.

The lifted-off contacts, however, are non-conductive. Depth-resolved x-ray photoelectron spectroscopy (XPS) measurements of the oxidation state of titanium near the metal-semiconductor interface for the metal-first contacts demonstrate a smooth transition from metallic Ti to fully-oxidized TiO_2 near the Ga_2O_3 surface (Figure 2a). In the lifted-off contacts, however, the oxidation state of Ti is far more disordered, and the Ti layer is not fully oxidized even at the Ga_2O_3 surface (Figure 2b).

This implies that liftoff processing can detrimentally modify the β-Ga_2O_3 surface and inhibit ohmic contact formation.

The metal-first process was then applied to fabricate TLM patterns with three ohmic (low Φ_M) metals (Al, Ti, and Cr). TLM measurements have linear-ohmic IV behavior for Al and Ti contacts, with highly-leaky Schottky behavior for Cr contacts due to the higher Φ_M. The Al contacts have an ultra-low contact resistance of 70 mΩ-mm, which is among the lowest reported values of Rc (Figure 3). Metal-first anode Schottky barrier diodes were also fabricated with three Schottky (high Φ_M) metals (Ni, Pd, and Pt). For the ohmic metals, Φ_B was extracted from the specific contact resistance using the thermionic field emission (TFE) model. For the Schottky metals, Φ_B was extracted from C-V, forward I-V fitting with the TFE model, and reverse I-V fitting with a numerical reverse leakage model developed by W. Li, et al [2]. The resulting barrier heights have a linear dependence on Φ_M with a slope of 0.46 and reasonable R2 value of 0.986, indicating that the Fermi-level is at least partially un-pinned by using metal-first contact processing to minimize damage or modification of the β-Ga_2O_3 surface (Figure 4).

Conclusions and Future Steps:

In this work, we demonstrate that metal-first contact processing decreases surface modification in β-Ga_2O_3 compared to liftoff processing and results in ultra-low non-alloyed contact resistances (70 mΩ-mm). Further, metal-first processing can at least partially un-pin the Fermi level in ohmic and Schottky contacts to β-Ga_2O_3, leading to an S value of 0.46. The surface orientation dependence of Fermi-level pinning bears further investigation, as this work included only a limited set of orientations, as does the temperature stability of these metal-first contacts, which is critical for high voltage device performance.

References:

[1] L. A. M. Lyle, J. Vac. Sci. Technol. A, 40, 060802 (2022).

[2] W. Li, D. Saraswat, Y. Long, K. Nomoto, D. Jena, and H. G. Xing, Appl. Phys. Lett., 116, 192101 (2020).

Transparent Dual Polarized Antenna

CNF Project Number: 2865-20
Principal Investigator(s): Amal El-Ghazaly[1]
User(s): Rabia Yahya[2], Haosen Yin[1], Amal El-Ghazaly[1]

Affiliation(s): 1. Electrical and Computer Engineering, Cornell University; 2. Department of Physics, Nouakchott University, Nouakchott, Mauritania

Primary Source(s) of Research Funding: NSF grant no. 2239066

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Research Group Website: vesl.ece.cornell.edu

Primary CNF Tools Used: ABM Contact Aligner, PV75 Sputtering System, Even/Odd Hour Evaporators

Abstract:

Herein, we present a novel transparent antenna with ultra-wideband (UWB) performance along with polarization diversity through four ports allowing MIMO operation. The antenna design can be of a great interest for a vehicular applications and Internet of Things (IOT) where the dual polarization and multiple ports allows as well as medical glasses and vehicular windows where transparency is needed for visibility. The proposed antenna provides compact size with dimensions of 50 mm x 50 mm, through the employment of CPW, dual orthogonal-polarization, isolation level of 20 dB, and envelope correlation coefficient (ECC) of 0.0016 as well as MIMO performance.

Summary of Research:

The structure of the proposed antenna, as shown in Figure 1, is a circular slot fed by four coplanar waveguide (CPW) lines through four semi-circular patches placed in a perpendicular arrangement to achieve orthogonal polarization. Four strips are inserted between the semi-circular patches to enhance the isolation between the ports and maximize the polarization purity of the antenna. The conductive layer of the antenna is composed of a thin film of Silver (Ag) inserted between two layers of Indium Tin Oxide (ITO). The conductor stack was deposited onto a glass substrate with approximate structure of ITO (48 nm)/Ag (17.5 nm)/ITO (42 nm)/ Glass (0.7 mm) as reported in [1], where a transparency of 88% and sheet resistance of 3.1 Ω/sq are achieved. A Corning Eagle XG glass substrate is used, having a relative permittivity of 5.27, loss tangent of 0.001, and thickness of 0.7 mm.

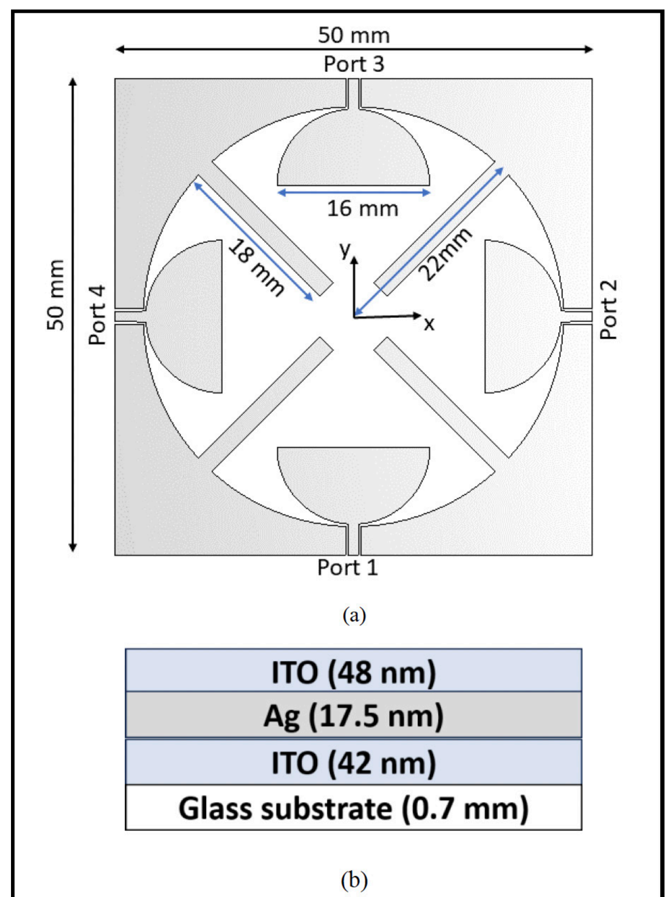

Figure 1: Structure of the proposed antenna. a) Perspective view and b) side view of the antenna design.

The proposed structure has been fabricated in the Cornell NanoScale Facility (CNF) and a picture of the fabricated antenna is included in Figure 2.

The fabrication process began by first, cleaning the glass substrate with acetone and isopropyl alcohol, then prebaking it before coating it with LOR-3A and S1813 photoresists. The antenna design was then exposed onto the substrate using a contact aligner and the pattern was developed. ITO was then sputtered onto the glass substrate on one side using an Indium-Tin target in a Kurt J. Lesker PVD 75 sputtering tool with a partial pressure of oxygen and a substrate temperature of 100°C. The composition of the ceramic sputtering target used is 90% Indium/10% Tin.

After sputtering the ITO, a layer of Ag with thickness of 17.5 nm was e-beam evaporated using a CHA evaporator. Later, the process of ITO deposition was repeated.

Subsequently, the substrate was soaked in Microposit Remover 1165 and sonicated to lift-off the photoresist and achieve the desired pattern. The substrate was then diced in a Disco wafer saw to extract the precise square antenna piece.

As a final step, 50 Ω SMA ports were connected to the antenna CPW feed lines using a conductive epoxy to prepare the antenna for measurement.

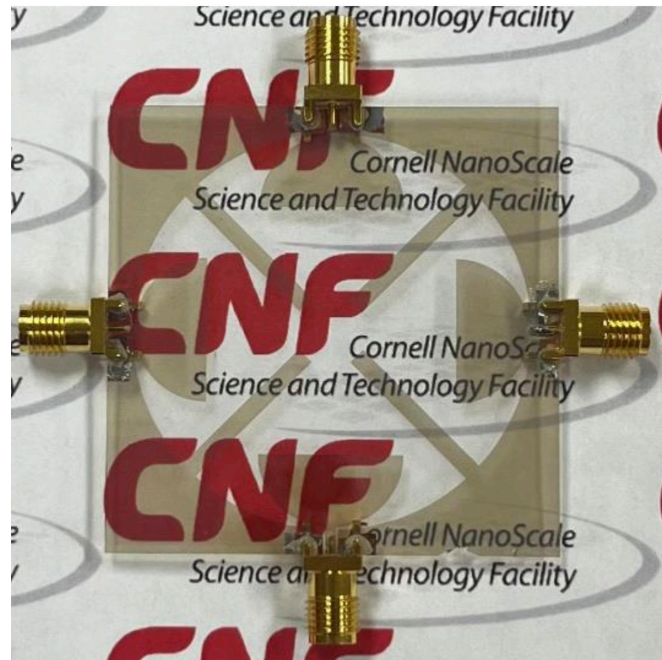

Figure 2: Image of the fabricated transparent antenna prototype.

Conclusions:

An ultra-wide band transparent antenna with features suitable for MIMO is proposed for various applications across automotive, IOT, and medical industries, among others. The performance of the antenna has been proven through simulation as well as primarily measurement results with return loss below -10 dB and an isolation level of 20 dB. The proposed antenna provides high transparency, a symmetric and compact structure, dual orthogonal polarization with similar radiation patterns, and diversity characteristics with ECC less than 0.0016 and DG on the order of 10 dB over the entire UWB.

References:

[1] J. -W. Kim, J. -I. Oh, K. -S. Kim, J. -W. Yu, K. -J. Jung and I. -N. Cho, "Efficiency-Improved UWB Transparent Antennas Using ITO/Ag/ITO Multilayer Electrode Films," IEEE Access, vol. 9, pp. 165385-165393, 2021, doi: 10.1109/ACCESS.2021.3131868.

ELECTRONICS

Superconducting Microwave Devices at the CNF

CNF Project Numbers: 2998-22, 3117-23
Principal Investigator(s): Valla Fatemi
User(s): Luojia Zhang, Haoran Lu, Kushagra Aggarwal, Saswata Roy

Affiliation(s): School of Applied and Engineering Physics, Cornell University

Primary Source(s) of Research Funding: Lab start-up account, AFOSR

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Research Group Website: https://fatemilab.aep.cornell.edu/

Primary CNF Tools Used: Heidelberg DWL2000, ABM contact aligner, AJA sputterer, AJA ion mill, Glen 1000, Angstrom e-beam deposition, both JEOL systems

Abstract:

The Fatemi Lab is interested in a spectrum of nanodevice research ranging from low dimensional materials to quantum circuits, with a focus on superconductivity, including novel superconductors or device physics enabled by superconductors. In the last year we have advanced our capability in superconducting qubit and resonator fabrication, as well as in graphene Josephson junctions.

Summary of Research:

We have developed high quality resonators and Josephson junctions for superconducting microwave qubits. With the transmon qubit and readout resonator fabricated partially at CNF, we demonstrated a new quantum control protocol [1]. We are also leveraging these skills to investigate novel materials and fabrication methods for superconducting qubits, aiming for higher performance.

Additionally, in our graphene mesoscopic superconductivity efforts, we have recently found that Ti/Al contacts deposited by e-beam evaporation have much higher contact transparency than Ti/Nb contacts deposited by magnetron sputtering. This could be due to work function mismatch or interface damage. We are continuing to investigate improved contacts by leveraging this observation. Preliminary Josephson devices, both two- and multi-terminal have been successfully tested in our lab.

Conclusions and Future Steps:

We have developed useful qubit and graphene Josephson junction fabrication at the CNF. Moving forward, we anticipate development of superconducting qubits and other novel microwave-frequency devices based on novel materials and graphene Josephson devices.

References:

[1] https://arxiv.org/abs/2405.15695

ELECTRONICS

System-on-Foil

CNF Project Number: 3028-22
Principal Investigator(s): Shane McMahon, Graeme Housser
User(s): Dylan Richmond, Marcus Gingerich, Chad Moore

Affiliation(s): Lux Semiconductors Inc.

Primary Source(s) of Research Funding: NSF SBIR Grants

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Research Group Website: luxsemiconductors.com

Primary CNF Tools Used: Electron-beam Evaporator (Odd & Even Hour), AJA Sputter, PT740, Trion III Minilock, SEM Supra & Ultra, Logitech CMP Orbis, Oxford PECVD, Heidelberg Mask Writer DWL2000, DISCO Dicing Saw, Oxford FlexAL, Savannah ALD

Abstract:

Lux Semiconductors is developing a new system-level advanced packaging technology, System-on-Foil, designed to overcome limitations of current packaging technologies. This architecture integrates a patterned metal core substrate, facilitating high-speed signal transmission between redistribution layers on the top and backside. Copper transmission lines are patterned in silicon wafer toolsets to achieve interposer-like densities, enabling high bandwidth, low latency routing for chiplet-based heterogeneous integration. The rigid metal substrate allows for thicker dielectric layers that enable low loss high speed transmission lines, leveraging the metal substrate as reference ground. High speed signal can be routed through the metal core in impedance matched coaxial vias with near zero crosstalk. The metal core also provides good thermal conductivity, CTE compatibility with silicon, and durability even in ultra-thin form factors.

Summary of Research:

Layers of circuitry containing oxides and metals are deposited and processed onto thin, metal wafers to realize interposer chiplets with 2.5D architecture. These chiplets act as intermediaries in the signal routing and delivery between transistor and PCB domains.

Conclusions and Future Steps:

We have realized thin, metal foil interposers, and integrated them with traditional and flexible hybrid electronics to demonstrate our technology. Our more recent work has been focused on increasing the number of layers with applications toward integrating high bandwidth memory with compute modules, photonics, and nurturing the chiplet ecosystem. Our future steps are to continue to deliver on our customer's needs. At the CNF, we look to learn and adapt to the challenges that are associated with layering thick oxides and metals together to achieve several-micron tall layer stacks. Development of our platform is also taking place at other NNCI institutions, such as Georgia Tech and U Penn.

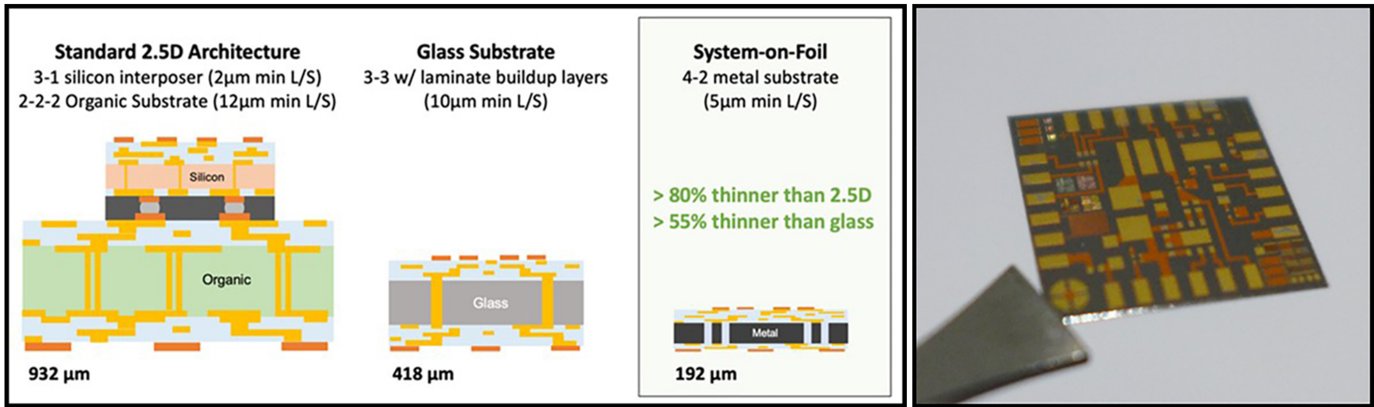

Figure 1: Advanced packaging cross sectional comparison.

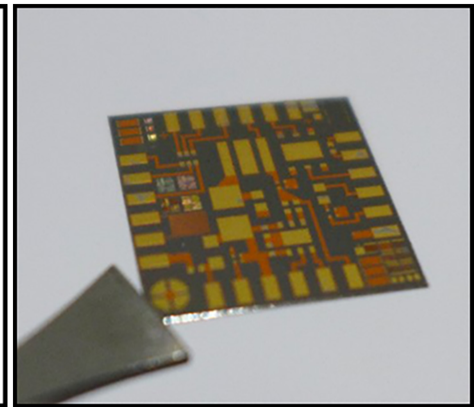

Figure 2: Completed metal foil interposer.

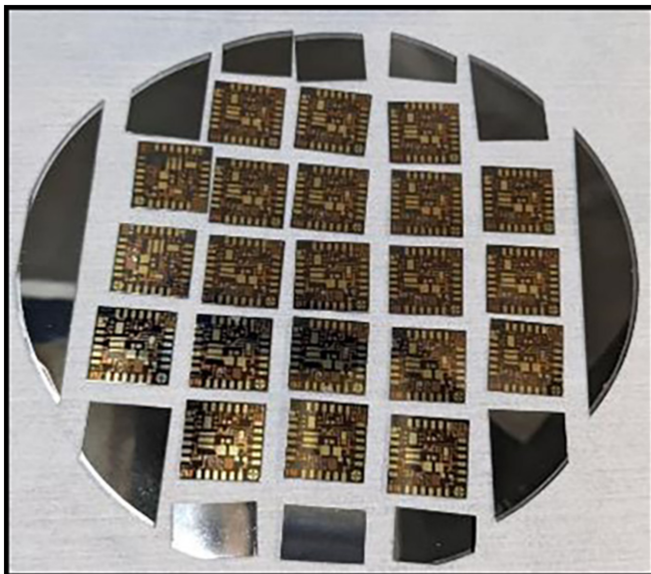

Figure 3: Completed 100 mm diameter metal foil substrate containing 21 interposers.

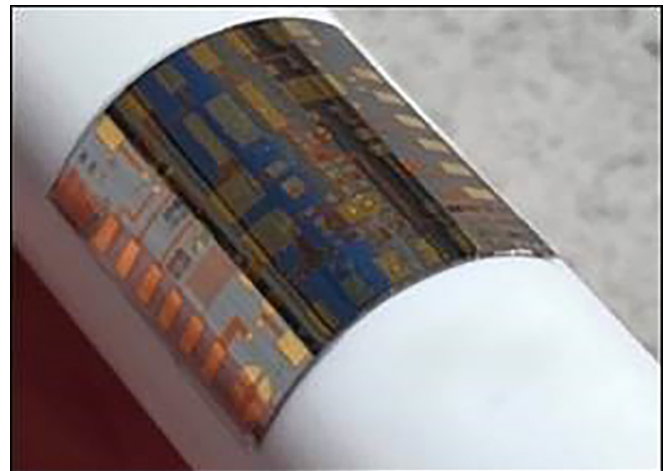

Figure 4: Metal foil interposer wrapped around a tube of Chapstick.

ELECTRONICS

ASIC Design for a Fast X-Ray Pixel Array Detector

CNF Project Number: 3065-23
Principal Investigator(s): Julia Thom-Levy
User(s): Nicholas Brown, Mark Tate, Sixuan Li

Affiliation(s): Laboratory of Atomic and Solid-State Physics, Cornell University

Primary Source(s) of Research Funding: United States Department of Energy

Contact: jt297@cornell.edu, njb234@cornell.edu, mwt5@cornell.edu, sl2536@corenll.edu

Primary CNF Tools Used: Cadence Virtuoso Software

Abstract:

The first Keck X-ray pixel array detector (Keck-PAD) was developed at Cornell University in the late 2000s. It is a high speed, high flux, photon burst detector that can take and store eight images at an image rate of roughly 10 MHz. It was designed to study fast condensed matter physics processes, such as crack propagation and materials failure, via x-ray diffraction at synchrotron storage ring x-ray sources, such as the Cornell High Energy Synchrotron Source (CHESS). However, synchrotron sources continue to advance in speed and brilliance thereby opening opportunities to study processes that require imaging at rates that exceed 10 MHz. Methods to create the K3 test chip (K3TC) — a chip with faster pixel electronics that follows in the footsteps of the original Keck detector — are presented in this report.

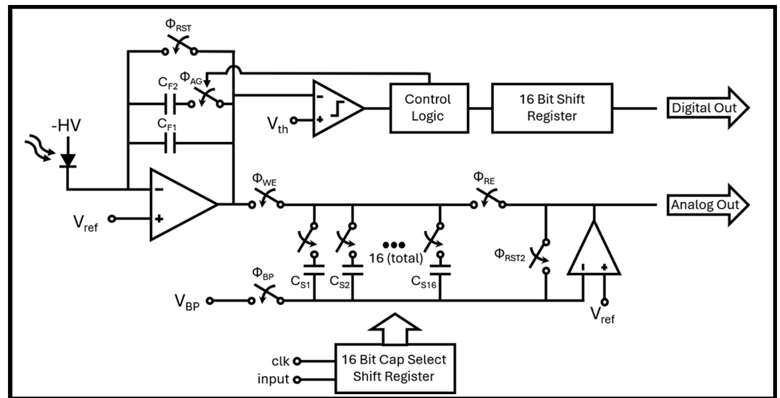

Figure 1: Block diagram of a single pixel for the K3TC.

Summary of Research:

The K3TC ASIC is organized as a 16 x 16 imaging array. A block diagram of the K3TC pixel can be seen in Figure 1. Incoming X-rays strike a semiconductor sensor, represented with a reverse biased diode in the diagram. This creates a correlated number of electron-hole pairs that are then separated by a large high voltage bias. K3TC can collect either electrons or holes, depending on the sensor. Once the charge has been collected, it is then integrated across CF1. A corresponding voltage is then produced at the output node of the amplifier. If this output voltage crosses an externally set threshold, VTH, then the pixel triggers adaptive gain, closing .AG, and adding more capacitance to the integrator. This, in turn, decreases the gain of the integrator, allowing it to collect more X-rays before saturating. At the end of an image the voltage is stored on a storage capacitor (CS1, CS2, etc.) and if the adaptive gain has been triggered, a digital "1" is added to the 16-bit shift register. The front end is then reset via .RST, and the next storage capacitor is switched in. The process is then repeated until all sixteen images have been taken.

After all sixteen images have been collected, the data is read off chip at a much slower rate. The analog and digital data is streamed from the chip in different channels and the analog data is converted to digital off chip. It is then passed into an FPGA, processed, and passed into a computer.

The first step of the current project was to identify the pain points in the previous Keck PAD. Real world tests found that the original Keck PAD could run at about 10 MHz (100ns per frame), but image quality began to break down at higher speeds [1]. Simulations performed in Cadence Virtuoso were used to identify limitations in the front-end amplifier and the reset switch. As can be seen in Figure 1, the design relies on an integrating op-amp, which needs to be fast to allow for the detector to keep up with all the large amount of signal. A new amplifier was drafted and simulated. It sacrifices DC gain for speed, while maintaining similar amounts of power draw. A new simple redesign of the reset switch reduced the on resistance, which speeds up resets.

Next, elements from another ASIC designed in the group, the Mixed-Mode PAD (MM-PAD) — a continuous imager designed for longer time scale, higher flux experiments than K3TC [2] — were incorporated and a K3TC test chip was submitted and fabricated in TSMCs 180 nm node size.

Conclusions and Next Steps:

A first step towards a fast X-ray pixel array detector was achieved, opening opportunities to study processes that require imaging at rates that exceed 10 MHz. A fast front-end amplifier was designed and a 16 x 16 pixel ASIC was fabricated in TSMC's 180 nm node size. Next, the functionality of the ASIC will be tested. For this purpose, a PCB has been developed to hold, power, and control parts of the chip. Data processing and finely tuned digital control will be done on an FPGA. Tests will focus primarily on speed, as well as noise performance, power consumption, and readout. Multiple test structures have been built into the chip and will be used to verify functionality of its components. Additionally, X-ray sensors will be bonded to the ASIC and tests will be conducted using optical pulsed lasers and X-rays sources.

References:

[1] L. Koerner, "X-ray analog pixel array detector for single synchrotron bunch time-resolved imaging," Cornell University, 2010.

[2] K. S. Shanks, Characterization of a Small-Scale Prototype Detector with Wide Dynamic Range for Time-Resolved High-Energy X-Ray Applications, Cornell University: IEEE, 2021.

Preferential Electrospray Deposition onto Interdigitated Electrodes

CNF Project Number: 3109-23
Principal Investigator(s): Paul Chiarot
User(s): Bryce Kingsley

Affiliation(s): Mechanical Engineering Department, State University of New York at Binghamton

Primary Source(s) of Research Funding: SUNY Binghamton IEEC Grant

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Research Group Website: https://sites.google.com/binghamton.edu/mmfl

Primary CNF Tools Used: AJA Sputter System(s), Heidelberg DWL2000, Hamatech Wafer Processor(s), SUSS MA6-BA6 Contact Aligner, YES Image Reversal Oven, YES Vapor Prime Oven, DISCO Dicing Saw, Photoresist Spinners/Hotplates

Abstract:

Electrospray deposition is an additive process that uses strong electric fields to atomize a liquid solution into a fine spray of charged microdroplets. Solute material dispensed in the liquid will be contained in the droplets, which undergo rapid in-flight solvent evaporation until dry particles of solute remain and are deposited on a surface to create a film. In this work, we investigate the preferentiality of electrospray deposition onto substrates with conductive and insulative components. Micro-scale devices were fabricated at the Cornell NanoScale Facility (CNF) that consisted of interdigitated metal electrodes on glass substrates. Fluorescent nano-particles were electrospray-deposited onto the devices and imaged with fluorescent microscopy to evaluate the preferentiality of deposition onto the conductive electrodes versus the insulative glass substrate.

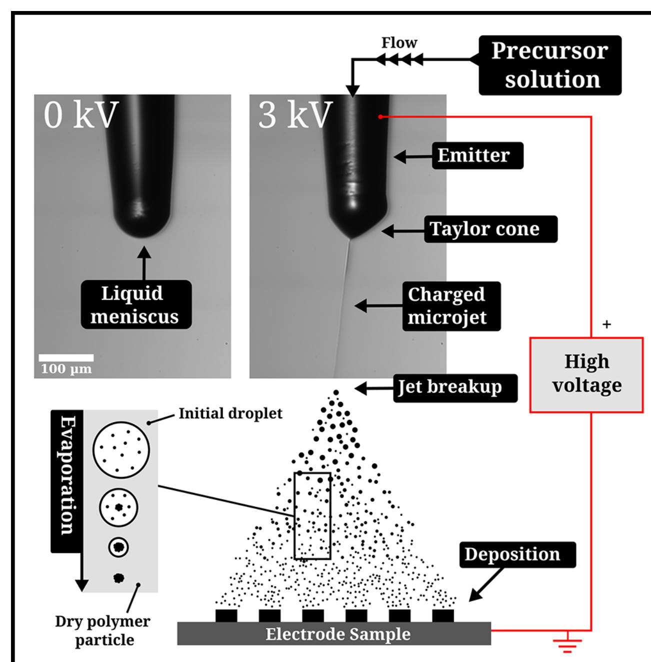

Figure 1: Schematic of electrospray deposition.

Summary of Research:

In this work we investigated the preferentiality of electrospray-deposited polymer films on multi-material substrates (i.e., substrates with conductive and insulative components). Figure 1 contains a schematic of the electrospray deposition process, which begins from a precursor solution composed of a solute material (polymer) in a volatile carrier solvent. The precursor solution is pumped through an emitter and charged with a high electric potential (3-5 kV) causing the liquid meniscus at the tip of the emitter to deform into a cone (Taylor Cone). A charged microjet is emitted from the tip of the conical meniscus which breaks up into a spray of nano- and micro-sized droplets. The volatile carrier solvent rapidly evaporates from the droplets, rendering a spray of dry (solvent-free) solute particles that are delivered to the substrate to create a film.

The deposition pattern of an electrospray is governed by the electric field formed between the emitter and the substrate. The charged droplets/particles follow the electric field lines to the target which preferably terminate on grounded conductive surfaces, allowing for preferential deposition of material onto conductive surfaces (versus neighboring insulative surfaces). In this work, we probed the geometric limits of preferential electrospray deposition by fabricating micro-scale devices at the CNF that were composed of interdigitated metal electrodes on glass substrates.

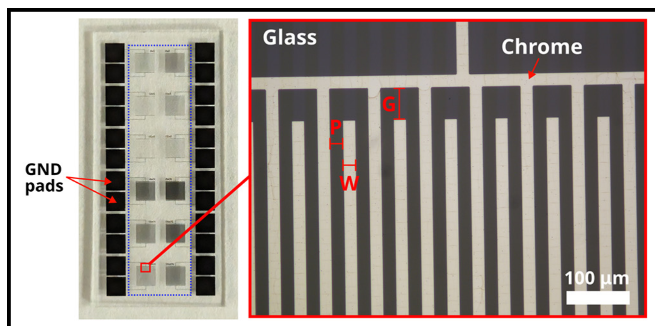

Figure 2: Optical and microscopic images of the electrode devices fabricated at CNF.

Figure 2 contains a photo and microscope image of a single device with 12 arrays of interdigitated chrome electrodes on a glass substrate. Each array on the device had a different electrode width (W) and pitch (P), with widths of 2, 5, 10, 20 μm and pitches of 5, 10, 20 μm. The microscope image outlined in red shows the 20 x 20 μm (WxP) array. All arrays used a uniform channel gap (G) of 50 μm. The interdigitated electrode devices were fabricated at the CNF.

The electrode pattern was designed using a python GDSII library (phidl) and converted to a mask using the mask writer at the CNF. Following mask fabrication, the device fabrication process was as follows: (1) sputter deposition of chrome (200 nm) onto glass substrate, (2) photoresist (S1805) spin-coating and baking, (3) expose with contact aligner, (4) NH3 image reversal, (5) flood exposure and develop, and (6) wet-etch chrome to reveal pattern.

The preferentiality of deposition onto the electrodes was evaluate by electrospraying fluorescent polystyrene nanoparticles (~ 100 nm diameter) and imaging with fluorescent microscopy. Figure 3 contains fluorescent microscope images of polystyrene deposition onto the electrodes. The image on the left is of the device that was fabricated (at CNF) using soda-lime (SL) glass as the substrate, and the device in the right image was fabricated on Borofloat (BF) glass. Notably, there is a significant difference in the deposition on the SL glass versus the BF glass. The device with SL glass (left) received a significantly greater amount of material on the glass substrate (the black area) compared to the device with BF glass (right) which received a minimal amount of material on the glass. The deposition onto the glass of the SL device (left) results in decreased coverage on the electrodes (outlined in red), as material is "lost" to the glass substrate. In contrast, the device with BF glass (right) has much greater coverage on the electrodes since less material was delivered (lost) to the glass substrate.

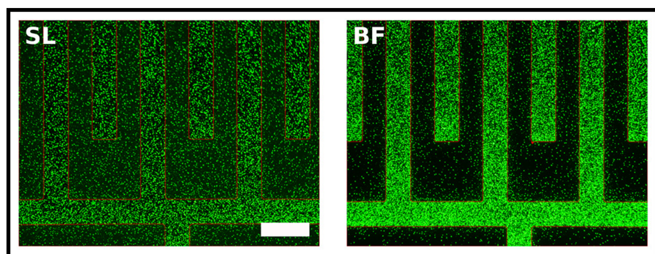

Figure 3: Fluorescent microscopy images showing the effect of glass substrate on preferentiality of electrospray deposition. Soda-lime glass is denoted by SL and Borofloat glass is denoted by BF. Scale bar in 40 µm.

Figure 4 plots the preference ratio (ratio of deposition onto electrodes vs. glass) versus metallization ratio (ratio area of electrodes vs. glass). Larger metallization ratios equate to electrodes with less glass area, resulting in preference ratios near or exceeding 0.9 (90%). Over all metallization ratios, the devices with BF glass substrate have greater preferentiality than those with SL glass. The difference in preferentiality between the SL and BF glass can be attributed differences in their dielectric properties. Electrospray deposition is highly sensitive to the electrical properties of the target material. For dielectric materials, the rate of charge decay governs the deposition onto the substrate. For preferential deposition, dielectrics with low rate of charge decay (BF glass) are beneficial as charge that is delivered (from the charged particles of the electrospray) to the surface of the dielectric will remain for a longer period of time and inhibit other charged particles from landing. Deposited charge will dissipate faster on dielectric with high charge decay (SL glass), resulting in greater accumulation of material on the glass.

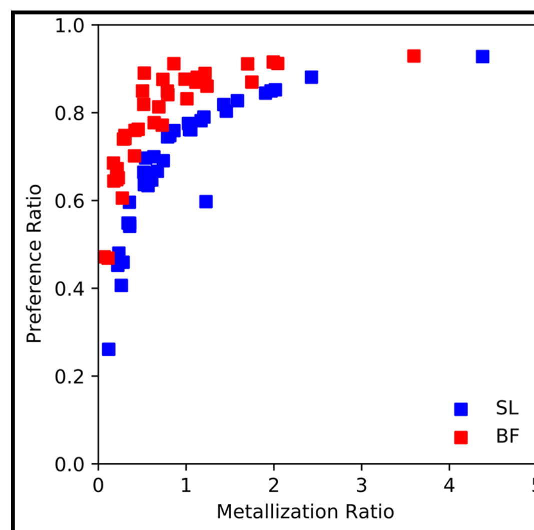

Figure 4. Plot of preference ratio vs. metallization ratio for SL glass (blue) and BF glass (red) substrates.