

# Development of Single and Double Layer Anti-Reflective Coatings for Astronomical Instruments

CNF Project Number: 2458-16

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Primary Source(s) of Research Funding: NASA Grant NNX16AC72G

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Primary CNF Tools Used: Oxford Plasma Enhanced Chemical Vapor Deposition,

Anatech Resist Strip, Oxford 81/82/100 Etchers, Manual Resist Spinners,

Resist Hot Strip Bath, Plasma-Therm Deep Silicon Etcher, ASML 300C DUV Stepper,

JEOL JBX 9500FS Electron-Beam Lithography System

## Abstract:

The Epoch of Reionization Spectrometer (EoR-Spec) is one of the instrument modules to be installed in the Prime-Cam receiver of the Fred Young Submillimeter Telescope (FYST). This six-meter aperture telescope will be built on Cerro Chajnantor in the Atacama Desert in Chile. EoR-Spec is designed to probe early star-forming regions by measuring the [CII] fine-structure lines between redshift  $z = 3.5$  and  $z = 8$  using the line intensity mapping technique. The module is equipped with a scanning Fabry-Perot interferometer (FPI) to achieve the spectral resolving power of about  $RP = 100$ . The FPI consists of two parallel and identical, highly reflective mirrors, forming a resonating cavity called etalon. The mirrors are silicon-based and patterned with double-layer metamaterial anti-reflection coatings (ARC) on one side and metal mesh reflectors on the other. The double-layer ARCs ensure a low reflectance at one substrate surface and help tailor the reflectance profile over the FPI bandwidth. Here we present the design and fabrication processes of silicon mirrors for the FPI.

## Summary of Research:

The goal of the project is to develop microfabricated, silicon-substrate-based mirrors for use in cryogenic Fabry-Perot Interferometers for astronomical instruments in the mid-infrared to sub-mm/mm wavelength regimes. The mirrors consist of high-purity, float-zone, 500- $\mu\text{m}$ -thick silicon wafers that are lithographically patterned with frequency-selective, gold mesh reflectors. Due to the high index of refraction of silicon, the other side of the mirror must be patterned with an ARC to achieve the broadband capability and mitigate contaminating resonances from the silicon surface [1,2].

The deep reactive-ion etching (DRIE) technique was employed to etch bulk silicon. It involves the Bosch processes which use alternate  $\text{SF}_6$  and  $\text{C}_4\text{F}_8$  gas exposures to produce near-vertical sidewalls and high aspect ratio features [3]. The fabrication recipe of the double-layer ARC structure is outlined in Figure 1.

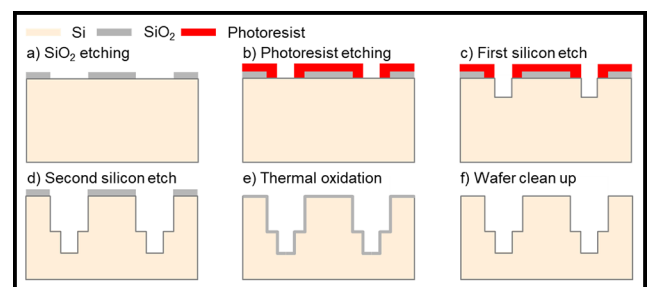


Figure 1: Key fabrication processes of the double-layer ARC structure.

Before performing DRIE silicon etches, we patterned  $\text{SiO}_2$  and photoresist grids as two silicon etch masks, defining the upper and lower geometry. Process (a) comprises three individual steps.

The SiO<sub>2</sub> layer was first deposited onto the wafer by an Oxford plasma-enhanced chemical vapor deposition (PECVD) machine. Another layer of UV photoresist was then printed above the SiO<sub>2</sub> using an ASML PAS 5500/300C DUV Wafer Stepper with a resolution of 0.2 μm, serving as the oxide etch mask. A final oxide etch in an Oxford inductively coupled plasma (ICP) dielectric etcher with O<sub>2</sub> and CHF<sub>3</sub> gases transferred the grid pattern from the photoresist to the SiO<sub>2</sub> layer. The photoresist residue was removed further in an O<sub>2</sub> asher. The other photoresist silicon etch mask was then spun and exposed by the same stepper mentioned before, shown in process (b).

After a short descum and seasoning process, we proceeded to do the first silicon etch using a Plasma-Therm DRIE deep silicon etcher. When the target depth was reached, the wafer was cleaned with an O<sub>2</sub> plasma for half an hour at 3000 W to remove the photoresist and C<sub>4</sub>F<sub>8</sub> related passivation residue. Then the second silicon etch was carried out, which constructed the upper ARC layer and pushed the lower ARC layer further down to the designated depths.

To further improve the morphology of the etched surfaces, we adopted a thermal oxidation and a clean-up process. We grew a sacrificial layer of thermal SiO<sub>2</sub> of about 1.1 μm thickness using water vapors at 1200°C for 100 mins in a furnace and then removed it by a hydrofluoric acid (HF) bath. The growth of the thermal SiO<sub>2</sub> layer and undercuts caused by previous etching processes widened the hole structure on both layers. Therefore, we shrank the dimensions on the mask designs by 1 to 2 μm accordingly to compensate for it. A scanning electron microscope (SEM) images of the double-layer ARC structure are shown in Figure 2.

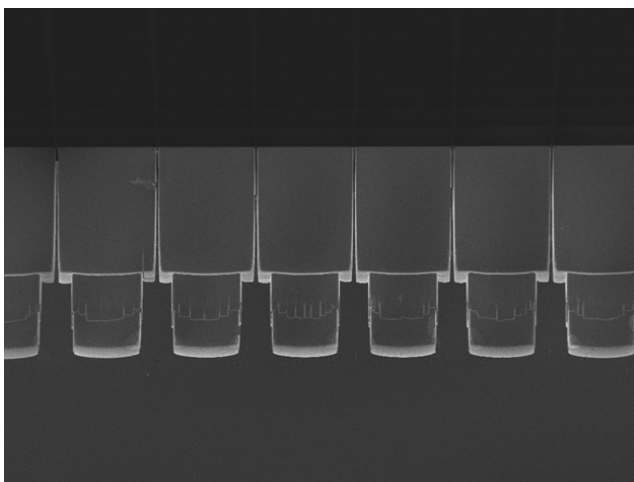


Figure 2: An SEM image showing the two-layer structure of anti-reflection coatings.

After constructing the double-layer ARC structure on one side of the silicon wafer, a layer of 2 μm photoresist was spun and baked on top of it to protect it from scratches and dust. Standard electron beam lithography, metal evaporation, and lift-off technologies were used to pattern the metal mesh structure on the other side. We coated the standard electron beam resist PMMA on the wafer and exposed it in a JEOL JBX 9500FS electron-beam lithography system with a maximum resolution of 6 nm. The wafer was then descummed and mounted inside a CVC SC4500 e-gun evaporation system where a 10 nm chromium adhesion layer and a 100 nm gold layer were evaporated. Afterward, we soaked the wafer into a Microposit 1165 remover bath heated to 80°C to lift the gold-coated PMMA layer off.

## Conclusions and Future Steps:

In the past year, we have refined our past recipes with electron-beam lithography to achieve better resolution. We have demonstrated our ability to fabricate double-layer ARCs for different wavelengths and metal meshes with different feature sizes. We also published a new paper [4] about the design and characterization of the silicon mirrors in SPIE.

Our next steps are to better characterize our etched geometries and improve our metamaterial ARCs using Fourier transform spectrometers, and then use the results to iterate on our fabrication design.

## References:

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