Nanotube Transistor Arrays on a TEM Substrate

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Primary CNF Tools Used: Low pressure chemical vapor deposition (LPCVD) furnaces (oxide, nitride), Autostep i-line stepper, ABM contact aligner, SC4500 evaporators, Oxford 80 RIE

Abstract:

We use photolithography to fabricate nanotube transistor devices on substrates with thin nitride windows, which can be imaged using transmission electron microscopy (TEM). Our device architecture permits us to characterize a given nanotube both electrically, and by high-resolution TEM. In low-dimensional systems, such as nanotubes, where nanoscale surface and defect structure can have profound influences on the electrical properties, we expect this combined nanoscale imaging and electrical characterization to yield insights that will inform the design of nanoscale sensors.

Summary of Research:

The study of low-dimensional materials, such as carbon nanotubes, graphene, and molybdenum disulfide, has been an area of growing interest over the past decades, in part due to their promise as molecular sensors. Due to their one-to-few-atom thickness, the properties of such materials often depend sensitively on surface adsorbates, substrate-surface interaction and defect structure. Improving sample cleanliness, for example, enabled the first observations of spin-orbit coupling in carbon nanotubes [1] and, more recently, the fractal quantum Hall effect, known as Hofstadter's butterfly, in graphene [2]. In order to understand these nanoscale structures and subsequently design improved sensors, a device architecture is needed that combines the atomic-level characterization afforded by TEM with the electronics characterization ability enabled by a gated, transistor-like geometry. We demonstrate that we can produce arrays of gated nanotube sensors devices, with reasonably high yield that can be characterized afterwards by TEM. Our design also keeps parasitic capacitance from our electrodes to the highly resistive silicon substrate low enough to enable electronic measurements of our transistors at MHz bandwidth.

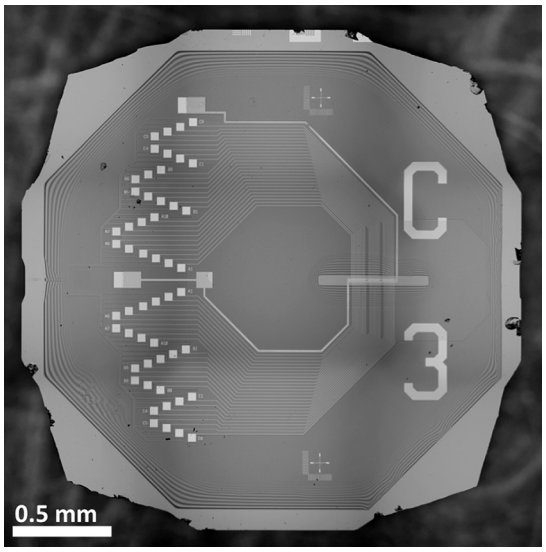

Figure 1: Optical image of microfabricated TEM grid with 26 pairs of source-drain electrodes, a top gate, and a thin nitride window for TEM imaging after top-gate is removed via chemical etching.

We fabricate nanotube devices on TEM grids using a combination of photolithography and standard nanotube growth and transfer techniques [3]. Figure 1 shows one of such devices, having 26 source-drain electrode pairs and two top gates. Between a few of the electrode pairs are individual nanotubes, which have been transferred prior to the deposition of a gate dielectric, and top-gate. The device fabrication involves using nine masks to define the various structures, which have been designed to yield nanotube devices with good gating characteristics, as well as low capacitive coupling between nearby electrodes.

The outline of the fabrication procedure is as follows. We begin by using low pressure chemical vapor deposition (LP CVD) to deposit the low-stress nitride on a 300 μm-thick silicon substrate, which will ultimately become our TEM window. We later deposit electrodes, and use

backside alignment followed by reactive ion etching (RIE) to expose rectangles on the back of the wafer which will later be used for a potassium hydroxide (KOH) through-etch. Arrays of parallel nanotubes are grown by CVD on a separate quartz substrate, coated with poly(methyl methacrylate) (PMMA), lifted off with KOH, and transferred onto the device substrate [3], where unwanted areas are patterned and etched using RIE. We use atomic layer deposition (ALD) to deposit a gate dielectric, after which we pattern and evaporate a gold top-gate. The surface is then coated with a KOH protection layer, and the devices are placed in hot KOH, which etches the silicon exposed on the back, to both release individual grids and to etch the silicon away from behind the nitride window. Later, the nanotube devices will be imaged through this window using TEM. The protection layer is then removed, and the grids are cleaned with oxygen plasma. Our fabrication process typically yields at least one electrically-connected, gated nanotube on 75% of the TEM grids.

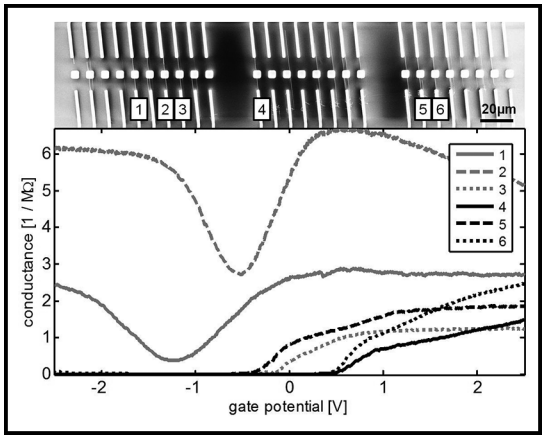

Figure 2: Upper: Scanning electron microscope image of nanotubes between source-drain electrodes, passing over thin nitride windows. Lower: Corresponding conductance measurements as a function of top gate voltage showing six conducting nanotubes with varying characteristics.

Figure 2 shows an SEM image of nanotubes patterned between the source-drain electrode pairs, imaged prior to top-gate deposition. The squares in the center are thin nitride windows for low-background TEM imaging. After completion of the device fabrication, these nanotubes are characterized electrically, shown in the lower portion of Figure 2. All of these nanotubes can be gated to have resistance lower than 1MΩ (50kΩ/μm) showing that they have a low defect density, and good coupling to the top gate. Nanotubes 1 and 2 can be seen to be metallic, while nanotubes 3-6 are semiconducting.

Furthermore, we can probe the electrical characteristics at high speeds in the megahertz (MHz) range. Previous research has shown that single charge fluctuations in a dielectric can be detected by semiconducting carbon

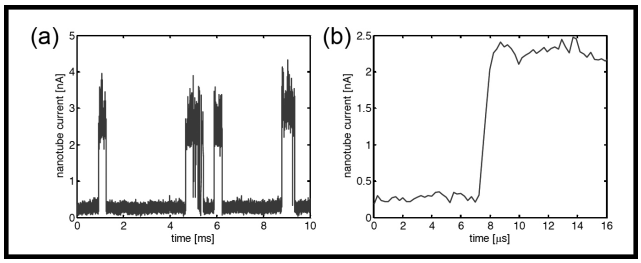

Figure 3: High-speed measurement of nanotube random telegraph signal showing (a) fluctuations in nanotube current and (b) measured rise time of less than 1 μs.

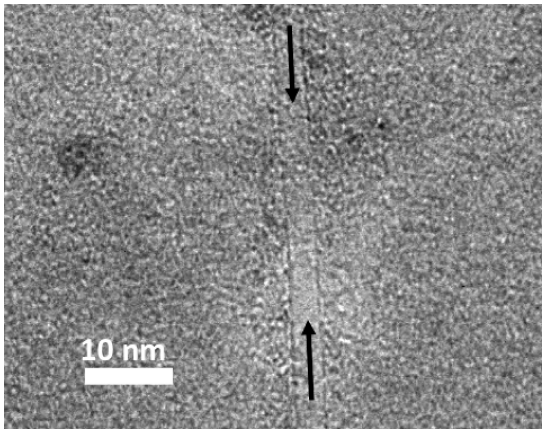

Figure 4: TEM image of a nanotube imaged through a thin nitride window, after top-gate removal.

nanotubes as random telegraph signals [4]. As shown in Figure 3, our devices are also capable of measuring such signals, but at higher speeds with rise times less than 1 μs. After characterizing the nanotubes electronically, we can etch away the gold top-gate, and image them by TEM to determine, for example, the nanotube diameter. Figure 3 shows one such nanotube, which can be seen to be single-walled (single dark lines running parallel to the arrows), and 4 nm in diameter (the width between those lines).

Conclusions and Future Steps:

In principle, our fabrication procedure can be applied to many different CVD-grown low-dimensional materials with only minor modifications, and may lead to the development of improved nanoscale sensors capable of high-speed molecular sensing.

References:

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