Organic Field Effect Transistor Fabrication

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Primary CNF Tools Used: Autostep i-line Stepper, Oxford 80+ Etcher, Oxford ALD FlexAL

Abstract:

We fabricated field-effect transistors with an integrated source-drain electrode silicon wafer with an improved liftoff process and an extra layer of hafnium dioxide (HfO_2).

Summary of Research:

Lead halide perovskites are an emerging class of semiconductors that have shown promising optoelectronic properties. The ability of lead-halide perovskites to maintain exemplary photovoltaic properties while being riddled with structural defects, mobile vacancies, and mobile ions make lead-halide perovskites unique and worth understanding in microscopic detail. Field-effect transistors (FETs) measurements combined with local Kelvin probe force microscopy is a powerful tool to microscopically study charge motion and charge injection in solution-processed semiconductors.

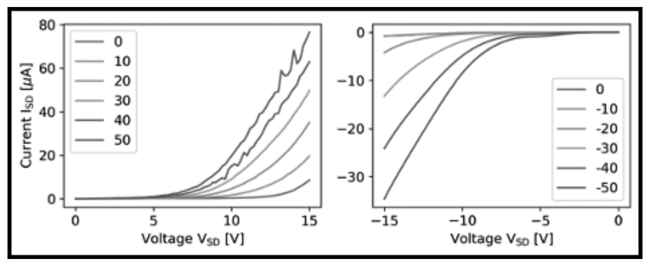

Figure 1: I-V curve for FET made from lead halide perovskite (FAMACs) on substrates fabricated at the CNF. Source-to-drain current (ISD) versus source-to-drain voltage (VSD) at different source-to-gate voltages (VG). Gate voltage sweep direction: 0 V to 50 V and 0 to -50 V.

The transistor substrates consist of gate pads and source-drain pads with interdigitated gold electrodes (5 nm Cr and 30 nm Au) with 5 µm spacing in between. The fabrication was previously developed [1] with a two-step exposure process on Autostep i-line stepper — the gate exposure layer (resist SPR 955 CM 2.1), and the source-drain exposure layer (resist nLOF 2020). The gate pads are etched using the Oxford 80+ etcher, and the gold electrodes are deposited with the odd-hour evaporator. The wafer undergoes a liftoff process and is diced on the DISCO dicing saw.

We have discovered several disadvantages of the previous protocol and improved the fabrication process.

We dramatically increase the yield of the transistors by employing a two-step liftoff process. After being submerged in Microposit Remover 1165 for 12 hours, the wafer is sonicated for six minutes with the solution, followed by a round of IPA spray and water blast cleaning. In the second step, the wafer was sonicated in methanol for three minutes to remove smaller metal particles, subsequently cleaned with IPA and water, and dried with N_2 and on hot plate at 110°C for 60 seconds. The yield improved from 57% to 95%, determined by if the source-drain is shorted due to metal remains on the electrodes.

However, bottom-gate bottom-contact perovskite FETs are difficult to successfully solution process and operate, presumably due to gate voltage induced ion motion and gate material induced material degradation from the widely used gate oxide SiO_2 [2].

Here, we modified and improved our existing FET substrate fabrication recipe to replace the SiO_2 gate with high-K material hafnium oxide, HfO_2, by atomic layer deposition (Oxford ALD FlexAL, 300°C, plasma, HfO_2, 200 cycles). The exposure time and focus are optimized.

We are still in the process of determining the improvement of the HfO_2 layer over the silicon oxide.

Triple cation lead halide perovskite (FAMACs) was solution-processed onto the resulting transistor substrates in a single step process in a glove box using published methods. The resulting films were annealed at 100°C for one hour. Transport properties were measured in the dark and under the vacuum of 5×10^6 mbar. The films showed a noticeable gate effect, which diminished under illumination and repeated measurements (Figure 1). More work is needed to improve the stability of the FETs and understand the effect of gate material and processing on the device performance.

References:

[1] Hoepker, N. C. "Fluctuations Near Thin Films of Polymers, Organic Photovoltaics, and Organic Semiconductors Probed by Electric Force Microscopy", 2013, Ph.D. thesis, Cornell University, Ithaca.

[2] Canicoba, N,. et al. "Halide Perovskite High-K Field Effect Transistors with Dynamically Reconfigurable Ambipolarity", ACS Materials Lett., 2019, 1, 633-640.