WSe_2 RF MOSFETs and CMOS Integration

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Primary CNF Tools Used: ABM contact aligner, Autostep I-line stepper, PT720-740 etcher, SC4500 odd-hour evaporator, P10 profilometer

Abstract:

We've demonstrated that it is practical and promising to integrate TMDs or other 2D materials into current CMOS process based on large-scale transferred CVD MoS_2, dispensed liquid-exfoliated MoS_2, and temperature assisted converted $PtSe_2$ [1-4]. Of all two-dimensional (2D) atomic-layered materials, WSe_2 is particularly attractive for electronic applications because it has a sizable bandgap, a high carrier mobility, and can be grown on large scale by chemical vapor deposition (CVD). Additionally, both p-type and n-type conductions have been demonstrated, making it possible to realize complimentary logic in WSe_2. In the present experiment, CVD-grown millimeter-sized WSe_2 flakes were etchant-free transferred onto Al gates covered by 30-nm-thick Al_2O_3 gate insulation. With Al_2O_3 passivation, the fabricated WSe_2 MOSFETs were found stable for more than five months. The Al_2O_3 passivation had the additional benefit of enhancing the current capacity of the MOSFETs by two orders of magnitude. Temperature-dependent small-signal microwave measurements showed that both the forward current-gain cut-off frequency (f_T, Figure 1a) and the maximum frequency of oscillation (f_{MAX}, Figure 1b) of the MOSFETs tend to peak near room temperature, with f_T ~ 600 MHz and f_{MAX} ~ 2 GHz (Figure 1c) [5].

Summary of Research:

Fabrication. The main difference of the fabrication between this work and [1] is in the material preparation part. In this work, multilayer tungsten diselenide (WSe_2) films were synthesized on c-plane sapphire substrate through a multi-step gas source chemical vapor deposition (CVD) process [6]. After CVD growth, the film was transferred onto the target chip by an etchant-free transfer method [7].

Passivation Result. The transfer curves of the device at row 5 column 8 (Device 0508) before and after passivation are shown in Figure 2(a). With passivation, the transfer curve, under drain-source bias (V_{DS}) of 1 V, shows current capacity increased by more than two orders of magnitude from ~ 1 nA/μm to ~ 200 nA/μm. Although the on/off ratio decreased, the resulting transconductance still increased from ~ 0.5 nS/μm to ~ 30 nS/μm. In five months, the transfer characteristics did not show noticeable change compared with the characteristics directly after passivation.

DC & RF Thermal Dependence. Figure 2(b) and (c) shows the output and transfer characteristics under different temperature ranging from 223 K to 373 K, of the device at row 3 column 10 (Device 0310). From Figure 2(b), higher temperature leads to saturation at lower V_{DS} because the increasing phonon scattering lowered the mobility and saturation velocity of the electrons. The drain current decreased with increasing temperature under the same biases. The output curves also indicated that when V_{DS} < 1 V, the device characteristics were dominated by large resistances, which were probably the contact resistances at drain and source. From Figure 2(c), with increasing temperature, the hysteresis first increased and then decreased until at 373 K, the device showed p-type conduction, which suggested that temperature as high as 373 K could effectively anneal the sample and even change the conduction carrier type.

Figure 1(a) and (b) show the current gain and power gain of Device 0310 separately after de-embedding under different temperature. The f_T and f_{MAX} peak near room temperature (Figure 1c). The reason f_T and f_{MAX} peak near room temperature is probably due to competing temperature effects. For example, contact resistance, carrier mobility, and saturation voltage all decrease with increasing temperature. These competing effects are being characterized and will be incorporated into a device model to evaluate their combined effect.

Future Direction. First, the uniformity of device performances across the same chip based on single CVD film can be improved. Other than film uniformity itself, direct growth should also help as in the transfer process, the stress introduced by wrinkles during transfer is different at different locations. Second, better interface can be formed if the process can be done in connected ultra-high vacuum (UHV) chambers. This can help to rule out the ambient environment effects in the analysis and make results more reproducible. Third, hexagonal boron nitride can be used as both dielectric and passivation buffer layer to offer better interface and possibly better thermal stability. Finally, introducing contact bias and gate-length dependence study to truly understand the 2D channel.

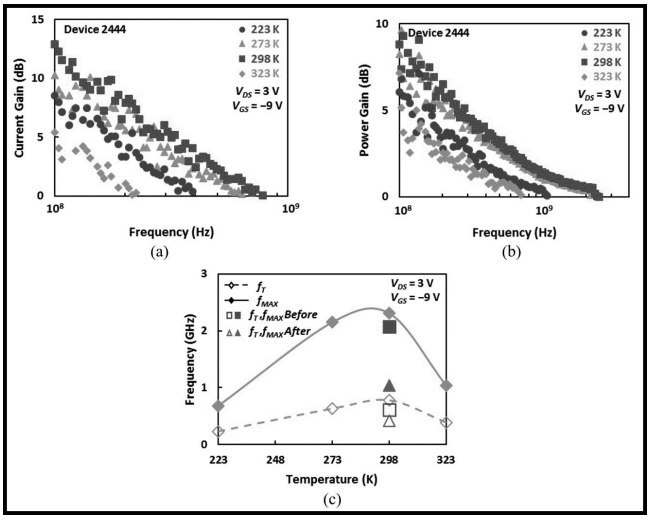

Figure 1: Temperature dependence of de-embedded small-signal (a) current gain, (b) power gain, and (c) cutoff frequencies. (Find full color on pages xiv-xv.)

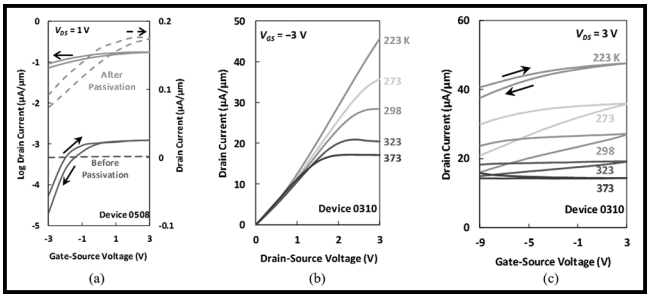

Figure 2: (a) Drain current under different gate-source voltages in log and linear scale, V_{DS} = 1 V, (b) output curves (V_{GS} = -3 V) and (c) transfer curves (V_{DS} = 3 V) of device 0310 under different temperatures (223, 273, 298, 323, 373 K).

References:

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