Reducing Write Current of Three Terminal Magnetic Tunnel Junctions by Engineering the Spin Hall Channel Structures

CNF Project Number: 111-80 Principal Investigator(s): Robert A. Buhrman User(s): Shengjie Shi

Affiliation(s): Applied and Engineering Physics, Cornell University Primary Source(s) of Research Funding: Department of Defense -Intelligence Advanced Research Projects Activity Contact: buhrman@cornell.edu, ss2882@cornell.edu Primary CNF Tools Used: ASML, JEOL e-beam 6300FS, Veeco AFM

Abstract:

Three terminal magnetic tunnel junctions (MTJs) are very good candidates for future cache memory applications due to their low energy consumption, fast switching characteristics, and reliable operation. To demonstrate the practicality of these structures being used in high density memory arrays, further reduced switching current is desired. In this report we show that by re-designing the layout of the spin Hall channel that is used to supply spin current that switches the MTJs, we can obtain significant reduction in switching voltage thanks to a dramatic decrease in the channel resistance caused by shortened length and a faster spread-out.

Summary of Research:

One of the key advances in magnetic memory technologies is the utilization of the giant spin Hall effect to switch a nanomagnet free layer in a magnetic tunnel junction (MTJ) structure. Due to the separate read and write channel, different aspects of the device can be engineered independently to satisfy different needs. We have shown that the reduction of Meff in the free layer can effectively reduce the switching current in the MTIs [1]. Another critical element of the MTJs is the spin Hall channel on which the switching voltage is applied where $V = I^*R_{channel}$. In order to further reduce the V needed to operate these MTJs, we now design a shorter and narrower channel that can scale down the $R_{\mbox{\tiny channel}}$ significantly (Figure 1) with the accurate exposure from the ASML. This has enabled lower V_{c0} compared to previously reported for similar structures [2]. Excellent write error rate shows that these devices can be reliably used with infinite endurance, which is advantageous over other type of emerging memory technologies (Figure 2).

References:

- [1] Shengjie Shi, Yongxi Ou, S. V. Aradhya, D. C. Ralph and R.A. Buhrman, Fast Low-Current Spin-Orbit-Torque Switching of Magnetic Tunnel Junctions through Atomic Modifications of the Free-Layer Interfaces. Phys. Rev. Applied. 9, 011002 (2018).
- [2] Aradhya, S. V., Rowlands, G. E., Oh, J., Ralph, D. C., and Buhrman, R. A. Nanosecond-Timescale Low Energy Switching of In-Plane Magnetic Tunnel Junctions through Dynamic Oersted-Field-Assisted Spin Hall Effect. Nano Lett. 16, 5987-5992 (2016).

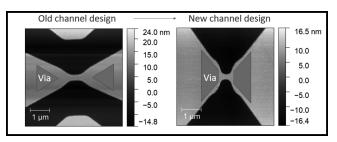


Figure 1: Schematic picture of the difference in the channel design.

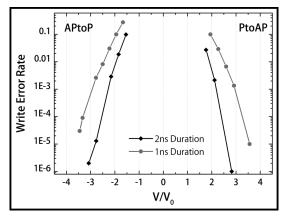


Figure 2: Write error rate measurement on a typical device made with the new mask design.