Vertical Tunneling Field Effect Transistors (Thin-TFETs) Based on BP/$SnSe_2$ Heterostructure

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Abstract:

Two-dimensional materials with clean surface and layered structure have many advantages over three-dimensional counterparts to be used for steep tunneling devices. This work presents two-dimensional heterojunction interlayer tunneling field effect transistors (Thin-TFETs) using black phosphorus (BP)/$SnSe_2$ heterostructure. Broken gap alignment (type III) between BP and $SnSe_2$ offers a desirable condition for band to band tunneling, and a solid polymer electrolyte (PEO:$CsClO_4$) is used to improve subthreshold swing. Graphite electrodes are used to protect air-sensitive BP surface, and most of processing is done in a glove box for the same reason. At room temperature in N_2, the subthreshold swing of the representative device reaches 180 mV/dec for exceeding two decades of drain current, and the I_{on}/I_{off} extends to more than three decades. This work helps the understanding of interband tunneling between layered materials, which forms the basis for low-power tunneling devices.

Summary of Research:

Two-dimensional materials with clean surfaces and layered structures have many advantages over three-dimensional counterparts to be used for steep tunneling devices. This work presents two-dimensional heterojunction interlayer tunneling field effect transistors (Thin-TFETs) using black phosphorus / tin selenide (BP/$SnSe_2$) heterostructure. Broken gap alignment (type III) between BP and $SnSe_2$ offers a desirable condition for band to band tunneling, and a solid polymer electrolyte (PEO:$CsClO_4$) is used to improve subthreshold swing. Graphite electrodes are used to protect air-sensitive BP surface, and most of processing is done in a glove box for the same reason. At room temperature in N_2, the subthreshold swing of the representative device reaches 180 mV/dec for exceeding two decades of drain current, and the I_{on}/I_{off} extends to more than three decades.

Figures 1 and 2 show the optical image of the representative BP/$SnSe_2$ TFET prior to the application of top-gate dielectric layer and the cross-sectional schematic image of the device. $SnSe_2$ flake was exfoliated onto a commercially available PDMS film and then transferred to a 285-nm-SiO_2/Si substrate. BP flakes were exfoliated onto another PDMS film and examined under microscope to estimate the layer thickness using optical contrast. The extreme air-sensitivity of BP poses a challenge when it is being exposed to the air during the metal electrode formation process.

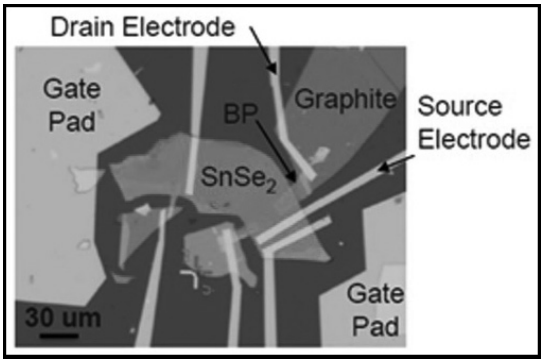

Figure 1: Optical image of the representative BP/$SnSe_2$ TFET.

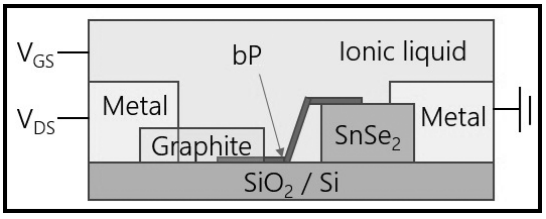

Figure 2: Cross-sectional schematic image of the device.

Semi-metallic graphite flakes were transferred on top of the BP flakes, which is used to make contacts with metal pads acting as a capping layer for BP. To minimize interfacial states resulting from interfacial damage or contamination, all the exfoliation processes were done in a glove box to protect air-sensitive BP and $SnSe_2$ from being exposed to the air. The substrate was spin-coated with e-beam resist in the glove box and Cr/Au electrodes (5/50 nm) were formed by e-beam lithography followed by lift-off in the glove box. The solid polymer electrolyte, PEO:$CsClO_4$, was deposited onto the substrate as a gate dielectric that also acts as a capping layer for BP and $SnSe_2$. When dissolved in PEO, $CsClO_4$ is ionized into Cs+ and ClO_4-, forming electric double layers which react to voltage bias.

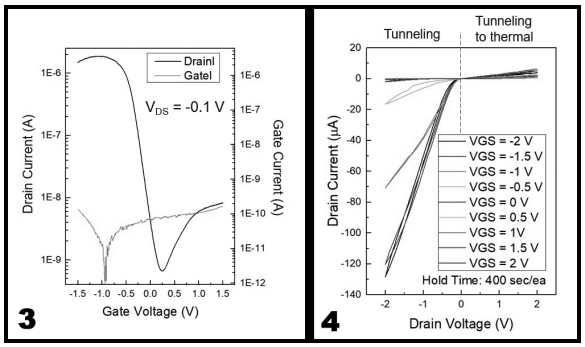

Figure 3, left: Current as a function of gate voltage at VDS = -0.1 V at room temperature in N_2. The black line indicates drain current and the red line indicates gate leakage current. Figure 4, right: Drain current as a function of drain voltage with different gate voltages.

The BP and $SnSe_2$ form type-III broken band alignment which is favorable to tunneling devices. Since $SnSe_2$ is degenerately doped, the band of BP can be selectively modulated by gate bias without the change in the band of $SnSe_2$, which allow to control the band offset between BP and $SnSe_2$. Figure 3 shows the representative transfer curve of the device when -0.1 V of drain bias is applied. (BP side is drain and $SnSe_2$ side is source.) This is to open the tunneling window between BP and $SnSe_2$ so that electrons in the valance band of BP can tunnel into the conduction band of $SnSe_2$. When the negative gate bias increases, the number of carriers in BP which can move to $SnSe_2$ side increases, resulting in the increase of drain current. When the positive gate bias increases, the portion of band to band tunneling decreases as the tunneling window gets smaller. If you keep increasing positive gate bias, the portion of conduction band to conduction band transport increases, and thus the drain current starts increasing. The transfer curve well explains the device characteristics of tunneling field effect transistors. Figure 4 shows the representative output curve of the device. Applying negative drain bias make the tunneling window size larger, increasing the difference between Fermi level of BP and $SnSe_2$. The drain current increases accordingly as shown in Figure 4. If positive drain bias is applied, the tunneling window decreases and the window get closed at some point. Increasing positive drain bias, however, enhance the thermionic emission of electrons from the conduction band of $SnSe_2$ to the conduction band of BP as in MOSFETS, leading to the increase of drain current in the opposite direction.

TFETs are said to have subthreshold swing less than 60 mV/dec in ideal case which is lower than so-called Boltzmann limit. In this case, however, the subthreshold swing is 180 mV/dec. The performance of tunneling devices is heavily dependent on interface properties such as interface trap density. If there exist many trap-density of states in the band gap, some portion of applied voltage will be lost to fill up those states. In addition, there is no negative differential resistance (NDR) observed in the output curve, which is one of the characteristic features of TFETs. This can be also attributed to the interfacial states. To see clear NDR behavior, the valley current should be small enough. If there are interfacial states, tunneling can happen even without tunneling window, which means inelastic current will increase the valley current. Electronic grade 2D material film growth as well as process to control interface quality should be developed to achieve high quality TFETs.

References:

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